2Gbit NAND Flash

Revision No.	History	Draft Date	Remark
Rev 00	Initial Draft	Feb. 2014	Preliminary
Rev01	Part number revise	Jul. 2015	

FEATURES SUMMARY

- **Single level cell technology**
- **OPEN NAND FLASH INTERFACE(ONFI) 1.0 COMPLIANT**

• POWER SUPPLY VOLTAGE

- VCC = 2.7V ~ 3.6V
- VCC = 1.7V ~ 1.95V

• MEMORY CELL ARRAY (with SPARE)

- Page size :

  x8 – 3.3V : (2K+64spare) bytes

  1.8V : (2K+128spare) bytes

- Block size :

  x8 – 3.3V : (128K+4Kspare) bytes

  1.8V : (128K+8Kspare) bytes

-. Device size : 2048blocks

• PAGE READ / PROGRAM TIME

- Random Read Time(tR) : 30us(Max)
- Sequential access time :
  3.3v - 25ns(Min),
  1.8V - 45ns(Min)
- Page program : 300us(Typ)

• BLOCK ERASE

- Block Erase Time : 3.5ms(Typ)

• COMMAND SET

- ONFI1.0 Compliant command set
- Read Unique ID

• SECURITY

- OTP area
- Serial number(unique ID)
- Non-volatile protection

• ELECTRONIC SIGNATURE

- 1st cycle: Manufacturer Code
- 2nd cycle: Device Code
- 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages, interleaved Program, Write Cache
- 4th cycle: Page size, Block size, Organization, Spare size, Serial access time
- 5th cycle : ECC, Multi-plane information

• RELIABILITY

- 50,000 Program / Erase cycles
  (with 4 bit ECC per 512 Byte)

• DATA RETENTION

- 10years

• Operating TEMPERATURE

- Commercial (0℃ ~ 70℃)
- Industrial (-40℃ ~ 85℃)

• CHIP ENABLE DON'T CARE OPTION

- Simple interface with microcontrollers

• PACKAGE OPTION

- Pb-Free Package

48-pin TSOP(12 x 20 / 0.5 mm pitch)

48-Ball FBGA: 6.5 x 8.0 x 1.0mm

63-Ball FBGA : 9.0 x 11.0 x 1.0mm

PRODUCT LIST

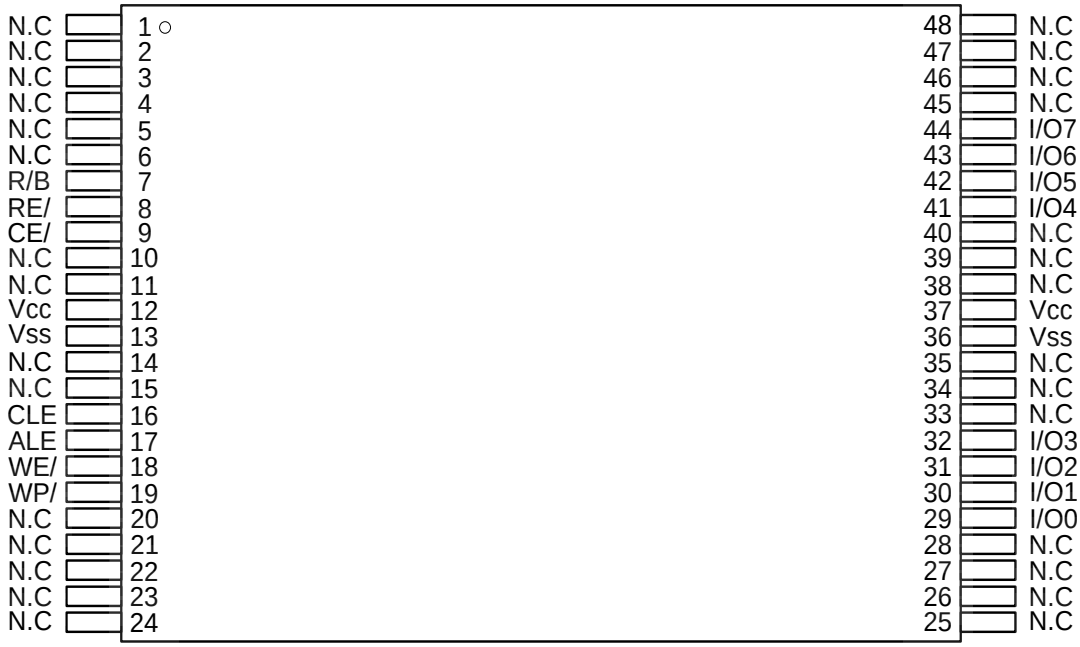
3.3V Product

Part number	Voltage	Bus Width	Package	Operating Temperature
AFND2G08U3A-CKA	2.7~3.6V	x8	12x20mm TSOP	Commercial
AFND2G08U3A-CKD			6.5x8.0mm FBGA	
AFND2G08U3A-CKE			9.0x11.0mm FBGA	
AFND2G08U3A-CKAI			12x20mm TSOP	Industrial
AFND2G08U3A-CKDI			6.5x8.0mm FBGA	
AFND2G08U3A-CKEI			9.0x11.0mm FBGA	

1.8V Product

Part number	Voltage	Bus Width	Package	Operating Temperature
AFND2G08S3-CKA	1.7~1.95V	x8	12x20mm TSOP	Commercial
AFND2G08S3-CKD			6.5x8.0mm FBGA	
AFND2G08S3-CKE			9.0x11.0mm FBGA	
AFND2G08S3-CKAI			12x20mm TSOP	Industrial
AFND2G08S3-CKDI			6.5x8.0mm FBGA	
AFND2G08S3-CKEI			9.0x11.0mm FBGA	

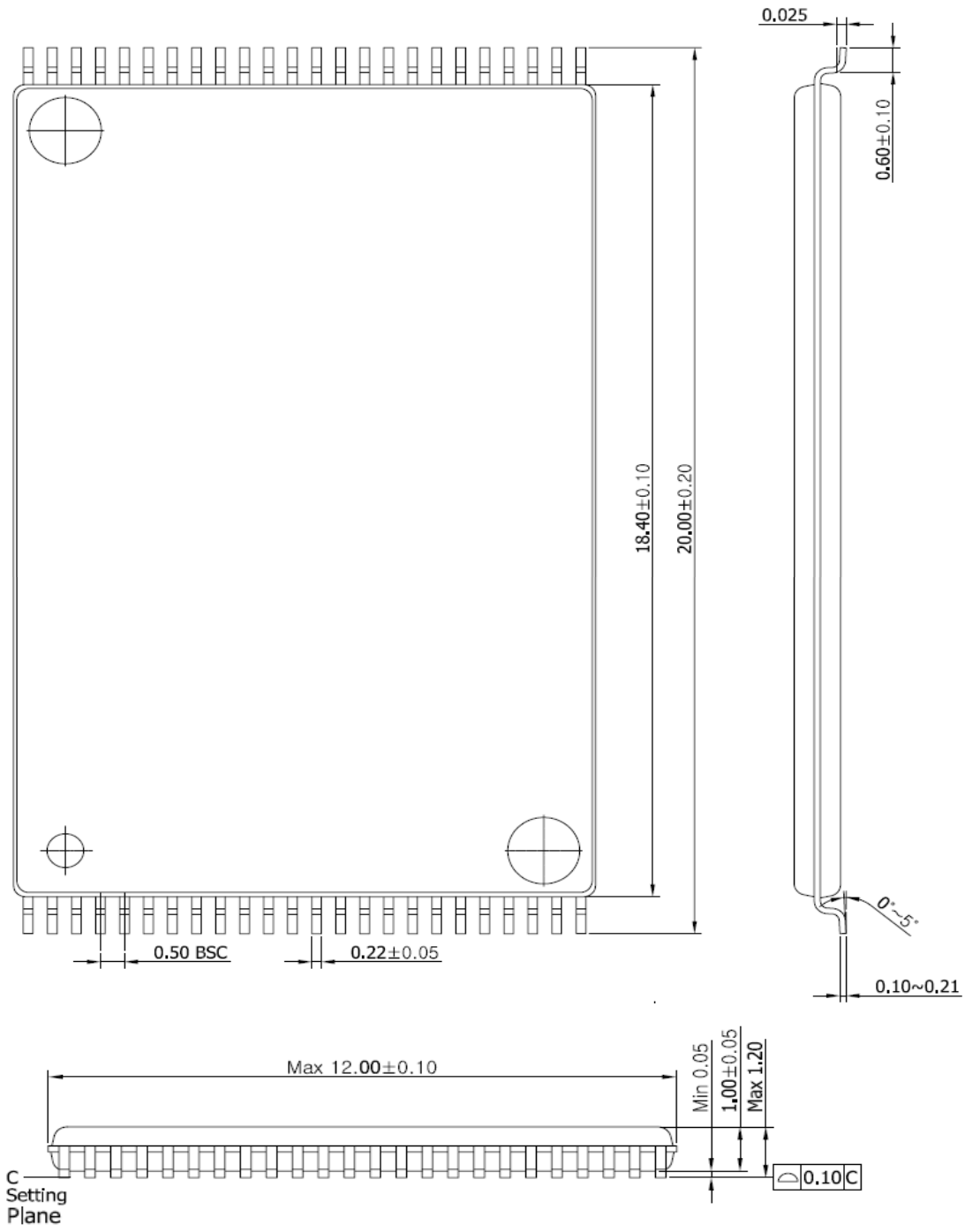
PIN CONFIGURATION (TSOP1)



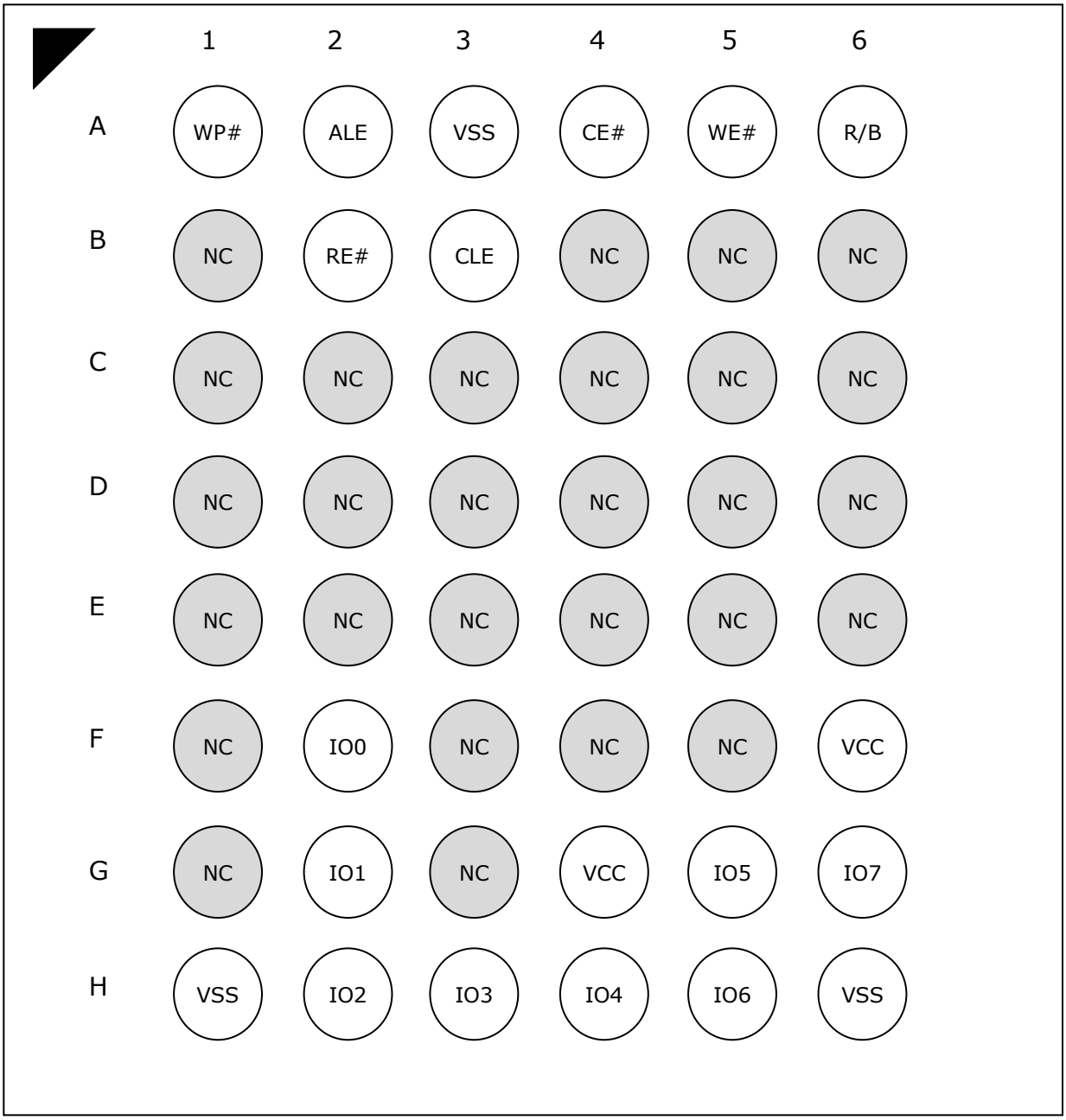
PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

Dimensions in millimeters

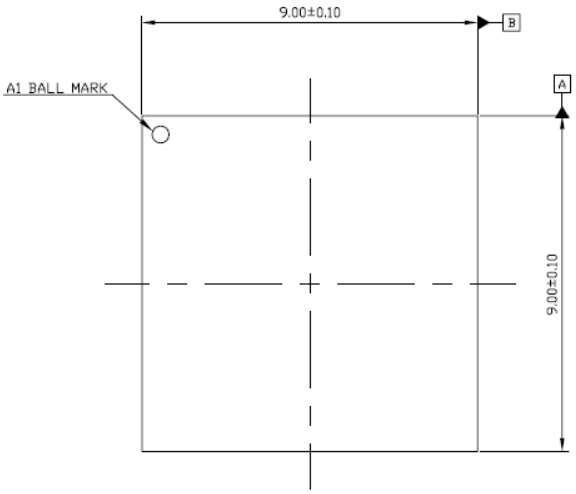


PIN CONFIGURATION (48ball-FBGA)

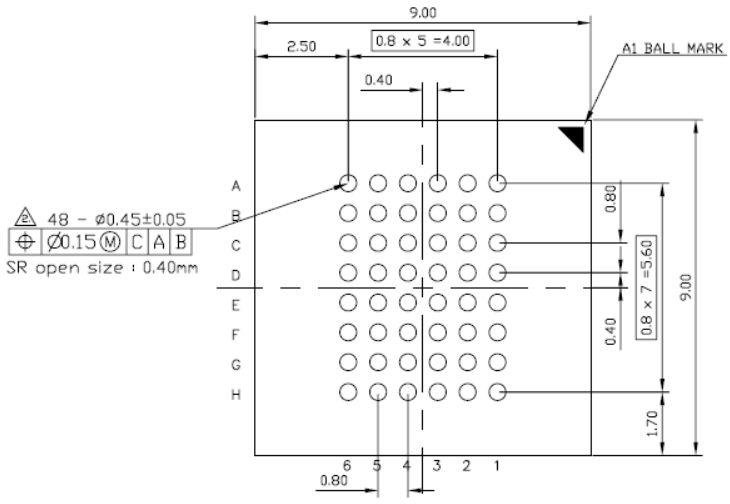


TOP VIEW

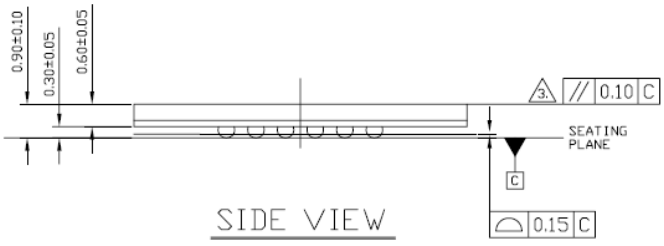
PACKAGE OUTLINE DRAWING (48ball-FBGA 9x9mm)



TOP VIEW



BOTTOM VIEW

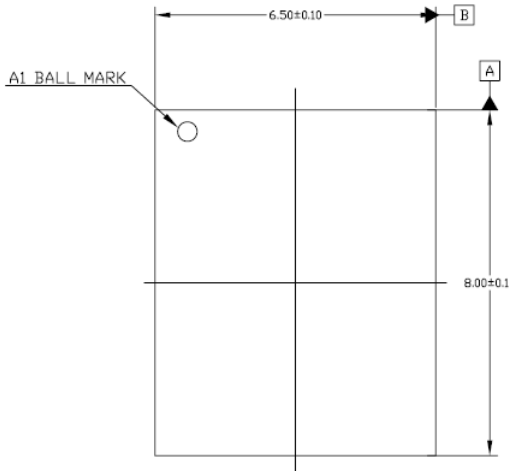


SIDE VIEW

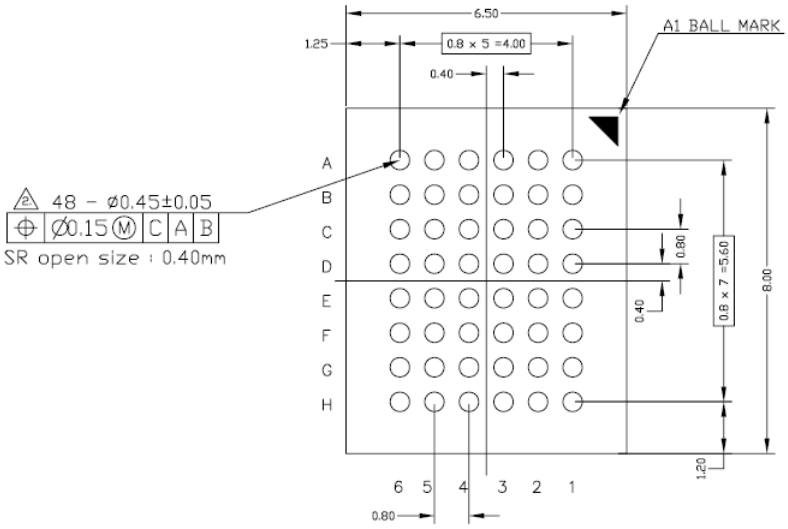
Description
FBGA 48BALL
Dimension
9.0mm x 9.0mm x 0.90mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

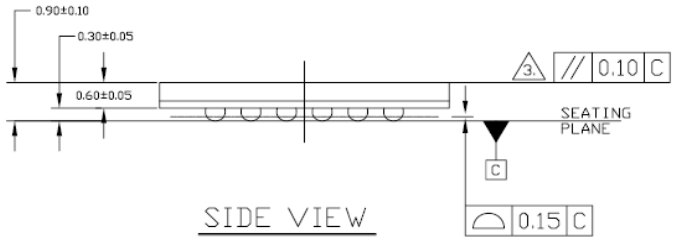
PACKAGE OUTLINE DRAWING (48ball-FBGA 6.5x8mm)



TOP VIEW



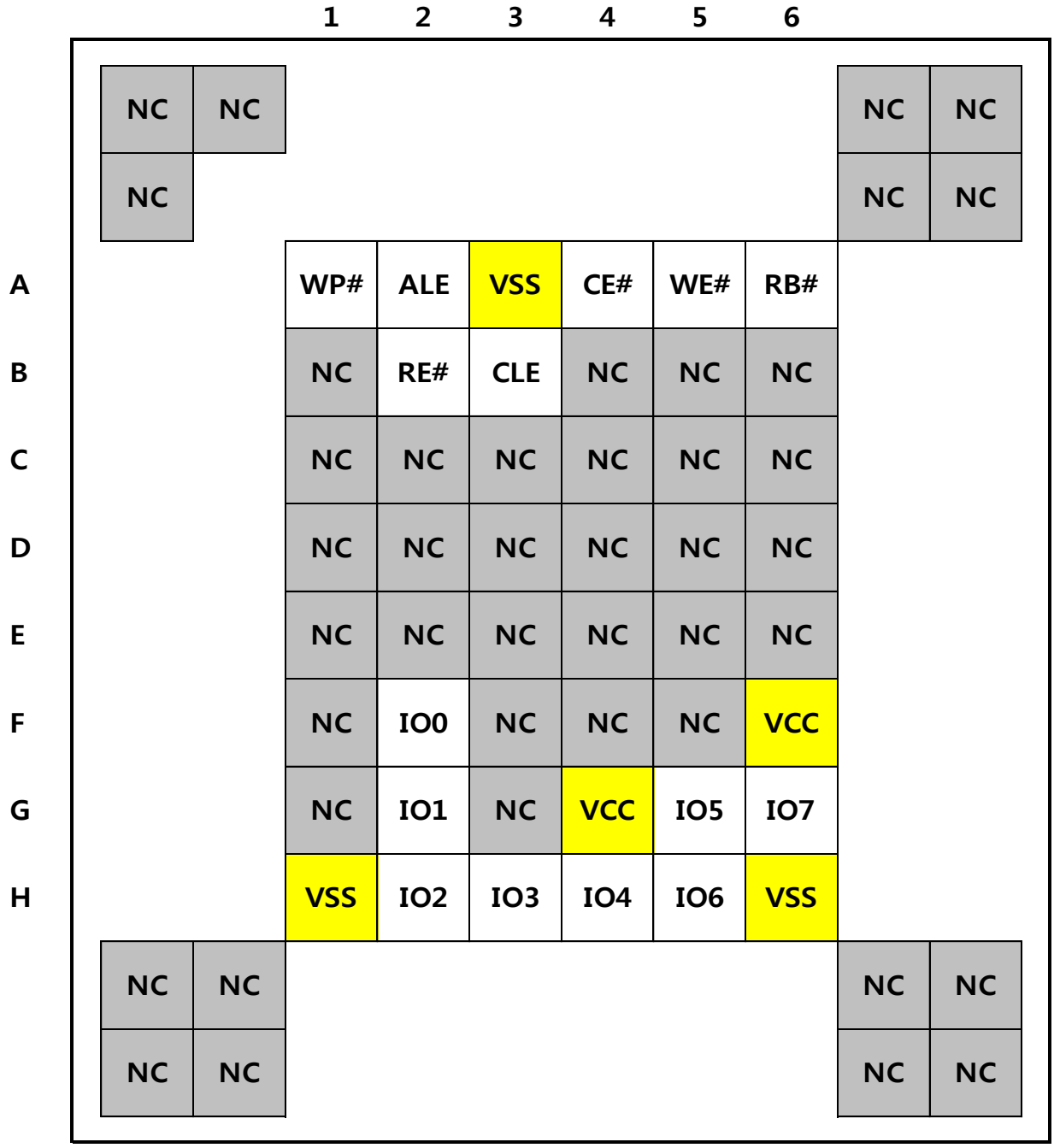
BOTTOM VIEW



Description
FBGA 48BALL
Dimension
6.5mm x 8.0mm x 0.90mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

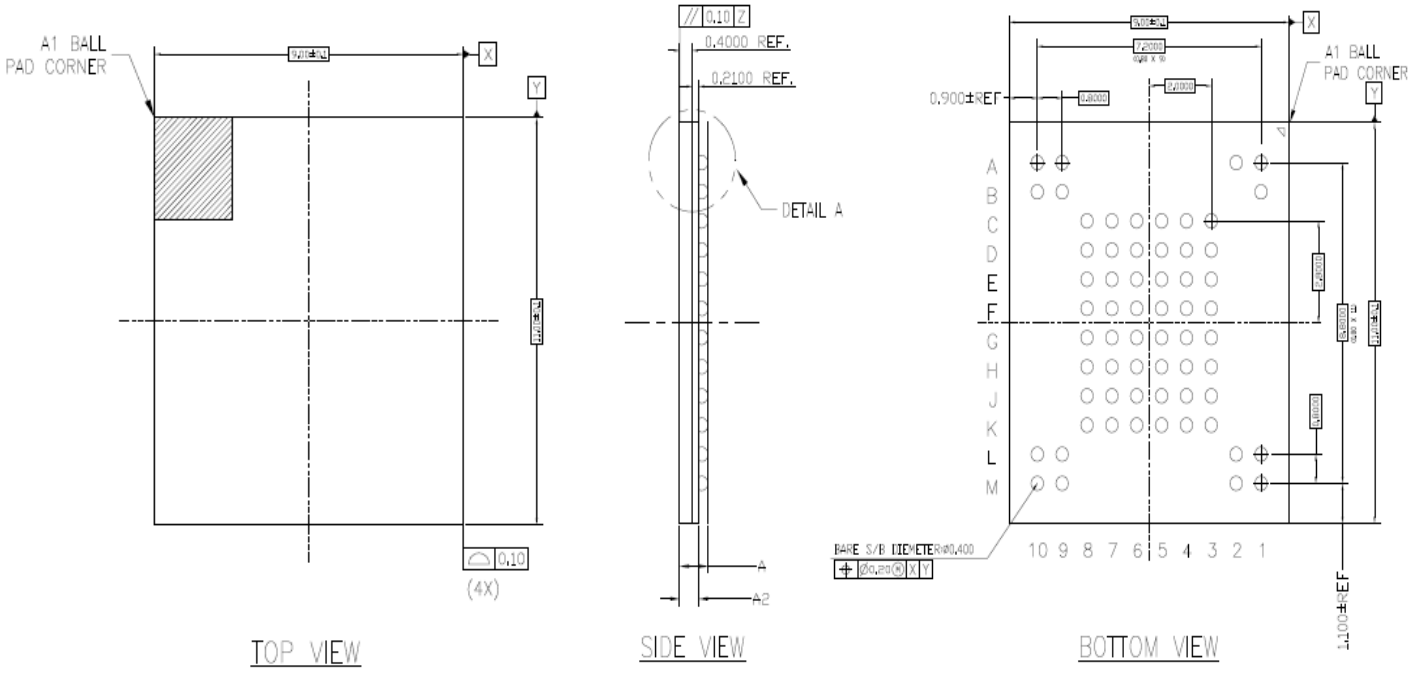
PIN CONFIGURATION (63ball-FBGA)

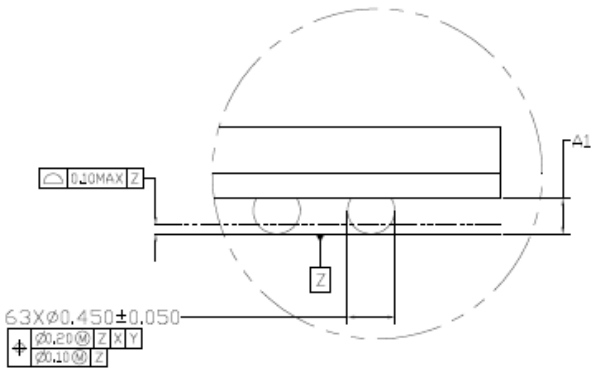


	1	2	3	4	5	6
	NC	NC			NC	NC
	NC				NC	NC
A		WP#	ALE	VSS	CE#	WE#	RB#	
B		NC	RE#	CLE	NC	NC	NC	
C		NC	NC	NC	NC	NC	NC	
D		NC	NC	NC	NC	NC	NC	
E		NC	NC	NC	NC	NC	NC	
F		NC	IO0	NC	NC	NC	VCC	
G		NC	IO1	NC	VCC	IO5	IO7	
H		VSS	IO2	IO3	IO4	IO6	VSS	
	NC	NC			NC	NC
	NC	NC			NC	NC

TOP VIEW

PACKAGE OUTLINE DRAWING (63ball-FBGA 9x11mm)





Description
FBGA 63BALL
Dimension
9.0mm x 11.0mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

1. SUMMARY DESCRIPTION

This NAND Flash is offered in 3.3/1.8 Vcc Power Supply, and with x8 and x16 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Depending on whether the devices have a x8 or x16 bus width, the page size is (2048 + 128 spare) bytes or (1024+64 spare) words. Each block can be programmed and erased up to 50,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND Flash devices, the implementation of an ECC is mandatory. The chip supports CE# don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.

In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages at a time (one per each plane) or to erase 2 blocks at a time (again, one per each plane). As a consequence, multi-plane architecture allows program/erase time to be reduced by 50%. The multi-plane operations are supported both with traditional and ONFI 1.0 protocols. Data in the page can be read out at 25ns (3V version) and 45nsec (1.8V version) cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data.

In addition, Device supports INFI 1.0 specification. The copy-back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. We don’t have EDC function in this device. A write protect pin is available to provide hardware protection against program and erase operations. The devices feature an open-drain ready/busy output that identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to connect to a single pull-up resistor.

The devices have a cache read feature that improves the read throughput for large files. During cache reading, the devices loads the data in a cache register while the previous data is transferred to the I/O buffers to be read. This feature is implemented according to ONFI 1.0 specification. The devices is available to support below three security features:

-OTP (one time programmable) area which is a restricted access area where sensitive data/code can be store permanently.
-Serial number(unique identifier) which allows the devices to be uniquely indentified.
-Non-volatile protection to lock sensible data permanently.
These security features are subject to an NDA (non-disclosure agreement) and are, therefore, not described in the datasheet.

1.1. Pin Description

Pin Name	Pin Function
I/O0 - I/O7 or I/O8 - I/O15	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
/CE	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, CE# low does not deselect the memory. The device goes into Stand-by mode when CE# goes High during the device is in Ready state. The CE# signal is ignored when device is in Busy state, and will not enter Standby mode even if the CE# goes high.
/RE	**READ ENABLE** The /RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of /RE which also increments the internal column address counter by one.
/WE	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
/WP	**WRITE PROTECT** The WP# pin, when Low, provides a hardware protection against undesired write operations. Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.
R/B	**READY/BUSY OUTPUT** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**POWER** The VCC supplies the power for all the operations. (Read, Write, and Erase).
VSS	**GROUND**
N.C	**NO CONNECTED / DON'T USE**

Table 1 : Signal descriptions

Note:
A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.2. Functional Block Diagram

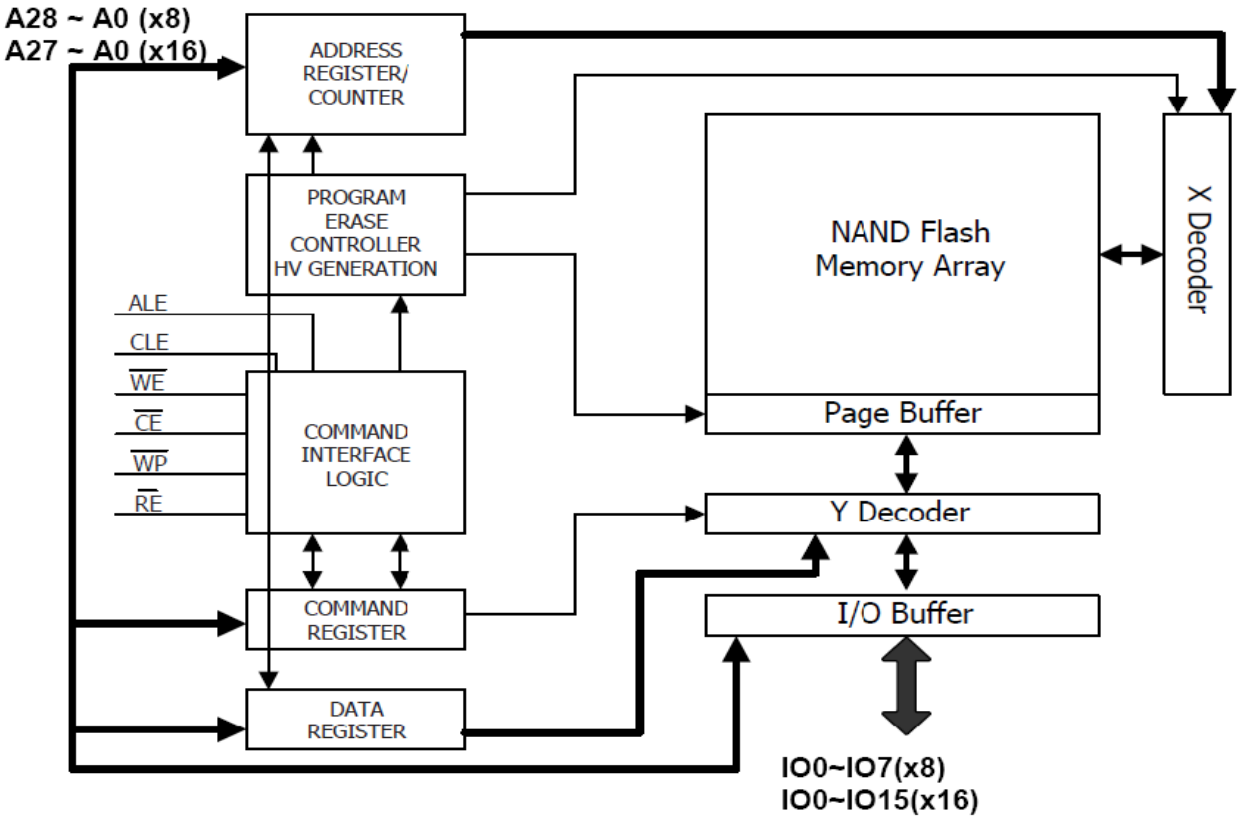


Figure 1 : Block diagram(SDP)

1.3. Array Organization

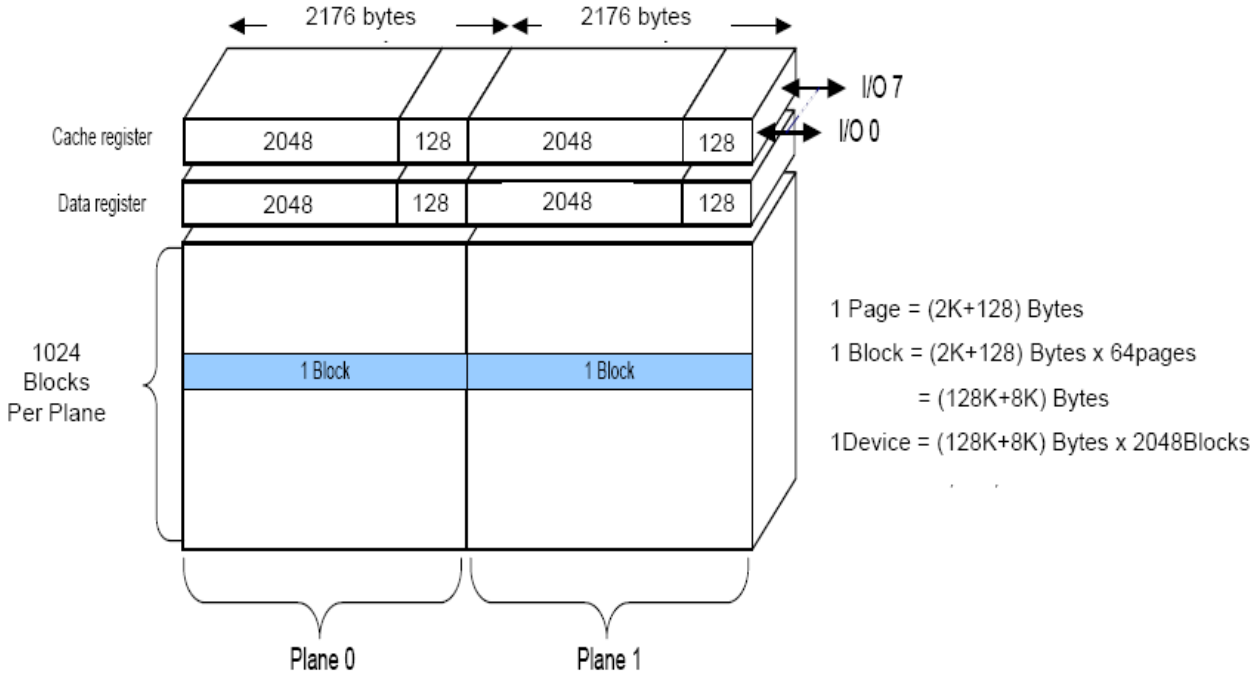


Figure 2 : Array organization(x8)

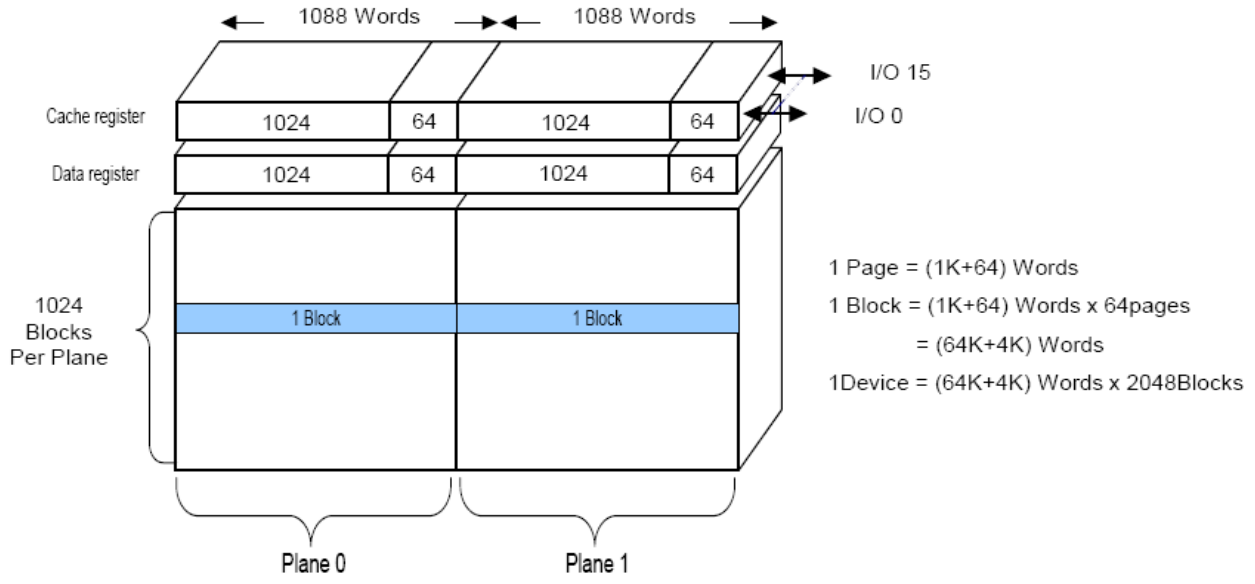


Figure 3 : Array organization(x16)

1.4. Addressing

1.4.1. Addressing(x8)

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th(*)Cycle	A28	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 2 : Address Cycle Map(x8)

As far as the address bits are concerned, the following rules apply:
A0 -A11 : column address in the page
A12 -A17 : page address in the block
A18 : plane address (for multi-plane operations) / block address (for normal operations)
A19 –A28 : block address

1.4.2. Addressing(x16)

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	L(1)	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26
5th(*)Cycle	A27	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 3 : Address Cycle Map(x16)

As far as the address bits are concerned, the following rules apply:
A0 -A10 : column address in the page
A11 -A16 : page address in the block
A17 : plane address (for multi-plane operations) / block address (for normal operations)
A18 –A27 : block address

Notes:
1. L must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st& 2ndcycle are Column Address, 3rdto 5thcycle are Row Address.
4. I/O 8 -I/O 15 must be L.

1.5. Command Set

FUNCTION	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable command during busy
PAGE READ	00h	30h	-	-	No
READ FOR COPY-BACK	00h	35h	-	-	No
SPECIAL READ FOR COPY-BACK	00h	36h	-	-	No
READ ID	90h	-	-	-	No
RESET	FFh	-	-	-	Yes
PAGE PROGRAM(Start) CACHE PROGRAM(End)	80h	10h	-	-	No
CACHE PROGRAM(Start)	80h	15h	-	-	No
PAGE RE-PROGRAM	8Bh	10h	-	-	No
COPY-BACK PROGRAM	85h	10h	-	-	No
(Traditional)MULTI-PLANE PROGRAM	80h	11h	81h	10h	No
ONFI MULTI-PLANE PROGRAM	**80h**	**11h**	**80h**	**10h**	**No**
MULTI-PLANE PAGE RE-PROGRAM	8Bh	11h	8Bh	10h	No
(Traditional)MULTI-PLAN (start/cont)	80h	11h	81h	15h	No
ONFI MULTI-PLANE CACHE PGM(start/cont)	**80h**	**11h**	**80h**	**15h**	**No**
(Traditional)MULTI-PLANE CACHE PGM(end)	80h	11h	81h	10h	No
ONFI MULTI-PLANE CACHE PGM(end)	**80h**	**11h**	**80h**	**10h**	**No**
(Traditional)MULTI-PLANE COPY-BACK PROGRAM	85h	11h	81h	10h	No
ONFI MULTI-PLANE COPY-BACK PROGRAM	**85h**	**11h**	**85h**	**10h**	**No**
BLOCK ERASE	60h	D0h	-	-	No
(Traditional)MULTI-PLANE BLOCK ERASE	60h	60h	D0h	-	No
ONFI MULTI-PLANE BLOCK ERASE	**60h**	**D1h**	**60h**	**D0h**	**No**
READ STATUS REGISTER	70h	-	-	-	Yes
READ STATUS ENHANCED	**78h**	**-**	**-**	**-**	**Yes**
RANDOM DATA INPUT	85h	-	-	-	No
RANDOM DATA OUTPUT	05h	E0h	-	-	No
CACHE READ (SEQUENTIAL)	31h	-	-	-	No
CACHE READ ENHANCED(RANDOM)	00h	31h	-	-	No
CACHE READ(End)	3Fh	-	-	-	No
READ PARAMETERPAGE	ECh	-	-	-	No

Table 4 : Command Set

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 Cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H [1)]	L	Rising	H	H		Address Input (5 Cycles)
L	L	L	Rising	H	H	Data Input	
L	L [1)]	L	H	Falling	X	Sequential Read and Data Output	
X	X	L	H	H	X	Data Output (suspended)	
L	L	L	H [3)]	H [3)]	X	During Read (Busy)	
X	X [1)]	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc [2)]	Stand-By	

Table 5 : Mode Selection

Notes:
1. X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and Multi-plane Read Status can be input to the device.

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. Typically glitches less than 5ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1. Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See "5.9. AC Timing Characteristics" for details of the timings requirements.

2.2. Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. (refer to "1.4. Addressing"). Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation(write/erase) the Write Protect pin must be high. See "5.9. AC Timing Characteristics" for details of the timings requirements.

2.3. Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See "5.9. AC Timing Characteristics" for details of the timings requirements.

2.4. Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See "5.9. AC Timing Characteristics" for details of the timings requirements.

2.5. Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6. Standby

In Standby the device is deselected, outputs are disabled and Power Consumption is reduced.

3. Device Operation

3.1. Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2176 bytes (x8) or 1088 (x16) of data within the selected page are transferred to the data registers in less than 30us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns (3V version) and 45nsec (1.8V version) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page.
After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.

3.2. Page Program

A page program cycle consists of a serial data loading period in which up to 2176 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks.
Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register.
Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.
The device is programmed basically by page, but it also allows multiple partial page programming of a word or consecutive bytes up to 2176 (x8) or 1088 (x16) in a single page program cycle.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. For example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

3.3. Page Re-program

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle.
On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm "10h". During page-re-program, address limitation applies as described in Figure 20 note 1 and 2 for copy-back function.
Similarly, the multi-plane page re-program allows to re-program two pages in parallel, one per each plane. The first page must be in the first plane while the second page must be in the second plane; the multi-plane page re-program operation is performed after a previously failed multi-plane page program operation. As for single page re-program case, multi-plane page re-program can be issued without any data manipulation.
During multi-plane page-re-program, address limitation applies as described in Figure 28 notes 1 and 2 for multi-plane copy-back function.

3.4. Multi-plane program

Device supports multi-plane program: it is possible to program 2 pages in parallel, one per each plane.
A multi-plane program cycle consists of a double serial data loading period in which up to 4352bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. Address for this page must be in the 1st plane(A18=0 for x8 devices, A17=0 for x16 devices). The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (tDBSY).
Once it has become ready again, either the traditional "81h" or the ONFI 1.0 "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be in the 2nd plane (A18=1 for x8 devices, A17=1 for x16 devices).Program Confirm command (10h) makes parallel programming of both pages to start. Figure 24 and Figure 25 describe the sequences.
User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program: read status register command is also available during Dummy Busy time (tDBSY).
In case of fail in any of 1st and 2nd page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "read status enhanced" command must be issued Refer to section 3.10 for further info.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

3.5. Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A18 to A28 are valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. See

3.6. Multi-plane Block Erase

Multi-plane erase, allows parallel erase of two blocks in parallel, one per each memory plane.
Two different command sequences are allowed in these case, traditional and ONFI 1.0.
In traditional case, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start. In this case, multi-plane erase does not need any Dummy Busy Time between 1st and 2nd block insertion.
As an alternative, the ONFI 1.0 multi-plane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multi-plane confirm). Between the two block-related sequences, a short busy time tIEBSYwill occur. Address limitation required for multi-plane program applies also to multi-plane erase. Also operation progress can be checked like in the multi-plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced.
As for multi-plane page program, the address of the first second page must be within the first plane (A18=0 for x8 devices, A17=0 for x16 devices) and second plane (A18 = 1 for devices, A17=1 for x16 devices), respectively.

3.7. Copy-back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2176 bytes(x8 Device) or 1088 words(x16 Device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or copy-back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 20"Copy-back Program with Random Data Input". When there is a program-failure at copy-back operation, error is reported by pass/fail status. But, if copy-back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, four bit error correction is recommended for the use of copy-back operation. Figure 20shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy-back, while it must be set to VccWhen performing the program. During copy-back operation, address limitation applies as described in Figure 20 notes 1 and 2.

3.8. Multi-plane copy-back Program

As for page program, device supports multi-plane copy-back program with exactly same sequence and limitations. Multi-plane copy-back program must be preceded by 2 single page read for copy-back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane). Multi-plane copy-back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.
Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) represented in Figure 28, and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h) represented in Figure 29 and Figure 30.
During multi-plane copy-back operation, address limitation applies as described in Figure 28 notes 1 and 2.

3.9. Special read for copy-back

The device feature the "special read for copy-back".
If copy-back read (described in sections 3.7 and 3.8) is triggered with confirm command "36h" instead "35h", copy-back read from target page(s) will be executed with an increased internal (Vpass) voltage.
This special feature is used in order to try to recover incorrigible ECC read errors due to over-program or read disturb: it shall be used ONLY if ECC read errors have occurred in the source page using "standard read" or "standard read for copy-back" sequences..
Excluding the copy-back read confirm command, all other features described in sections 3.7 and 3.8 for standard copy-back remain valid (including the figures referred to in those sections).

3.10. Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to
be toggled for updated status. Refer to "Table 7. Status Register Coding" for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

3.11. Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation on a specific plane in case of multi-plane operations.
Figure 11B defines the Read Status Enhanced behavior and timings. The plane address must be specified in the command sequence in order to retrieve the status of the plane of interest.
Refer to Table 7. for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.
Status register is dynamic in other words, user is not required to toggle RE# / CE# to update it.

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program	Coding
0	Pass / Fail	Pass / Fail	N/A	N/A	Pass / Fail (N)	N page Pass : '0' Fail : '1'
1	N/A	N/A	N/A	N/A	Pass / Fail (N-1)	N -1 page Pass : '0' Fail : '1'
2	N/A	N/A	N/A	N/A	N/A	-
3	N/A	N/A	N/A	N/A	N/A	-
4	N/A	N/A	N/A	N/A	N/A	-
5	Ready / Busy	Ready / Busy	Ready / Busy	P/E/R Controller Bit	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	N/A	Write Protect	Protected : '0' Not Protected : '1'

Table 6 : Status Register Coding

Notes:

1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2. I/O1: This bit is only valid for Cache Program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache Program sequence. When Cache Program is not supported, this bit is not used.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4. I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the last operation is complete.

3.12. Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to table 7 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for tRST after the Reset command is written..

3.13. Cache Read(available only within a block)

The Cache Read Sequential and Cache Read Random functions permit a page to be read from the page register while another page is simultaneously read from the Flash array. A Page Read command, as defined in table 5, shall be issued prior to the initial Cache Read Sequential or Cache Read Random command in a Cache Read sequence. A Cache Read Sequential or Cache Read Random command shall be issued prior to a Cache Read End (3Fh) command being issued.
The Cache Read (Sequential or Random) function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Cache Read (Sequential or Random) function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache Read (Sequential or Random) function. Issuing an additional Cache Read (Sequential or Random) function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a Cache Read Sequential (31h) command after the last page of the block is read. Figure 15defines the Cache Read behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. During Cache Read operation the only acceptable commands are Read Status, Random Data Output and Reset.

3.14. Cache Program (available only within a block)

Cache Program is used to improve the program throughput by programming data using the cache register(Figure 21). The Cache Program operation can only be used only within one block. The cache register allows new data to be input while the previous data that was transferred to the page buffer is programmed into the memory array. After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence (80h-15h). The Busy time following the first sequence 80h-15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model. In case of any subsequent sequence 80h-15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCBSYW). Read Status commands (70h) may be issued to check the status of the different registers, and the pass/ fail status of the Cache Program operations. More in detail: a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data. b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete. c) the Cache Program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in Cache Program operation. The latter can be polled upon I/O<6> status bit changing to "1" . d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while pro-gramming page N. The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation. See “table7. Status Register Coding".

3.15. Multi-plane Cache Program

The device supports Multi-plane Cache Program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache. The device supports both the traditional and ONFI 1.0 command sets.

The command sequence can be summarized as follows:

a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A18=0 for x8 devices, A17=0 for x16 devices). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.

b) The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

c) Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A18=1 for x8 devices, A17=1 for x16 devices). The data of 2nd page other than those to be programmed do not need to be loaded.

d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence.

   The sequence 80h-...-11h...-...81h...-...15h (or the corresponding ONFI 80h-...-11h...-...80h...-...15h) can be iterated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.

   The sequence to end Multi-plane Cache Program is 80h-...-11h...-...81h...-...10h (or 80h-...-11h...-...80h...-...10h for the ONFI 1.0 case).Figure 31and Figure 32 show the command sequence for the Multi-plane Cache Program operation for the two protocols. Multi-plane Cache Program is available only within two paired blocks belonging to the two planes.

   User can check operation status by R/B# pin or read status register commands (70h or 78h)If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes. More in detail:

a) I/O<6> indicates when both cache registers are ready to accept new data.

b) I/O<5> indicates when the cell programming of the current data registers is complete)

c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1".

d) d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".

   If the system monitor the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

3.16. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Figure 16 shows the command sequence.
The 5-byte Read ID configuration are supported: The device operating mode (5-byte) is selected through cam setting.

3.16.1. Legacy Read ID

Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 16 shows the operation sequence, while Table 8 to Table 12 explain the byte meaning. Complete read id code table is as follows.

Parameter	Symbol
Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
4th	Page size, Block size, Spare Size, Organization, Serial Acces time
5th	ECC, Multi-plane information

Table 7 : "Legacy" Read ID bytes meaning

3.16.2. Read ID Data Table(5cycle)

Density	Voltage (Vcc)	Bus Width	Manufacture Code	Device Code	3rd	4th	5th
2Gbit	3.3V	x8	ADh	DAh	90h	95h	46h
	3.3V	x16	ADh	CAh	90h	D5h	46h
	1.8V (128Byte spare)	x8	ADh	AAh	90h	15h	46h
	1.8V (128Byte spare)	x16	ADh	BAh	90h	55h	46h
	1.8V (64Byte spare)	x8	ADh	AAh	90h	11h	46h
	1.8V (64Byte spare)	x16	ADh	BAh	90h	51h	46h

Table 8 : Legacy " Read ID for supported configurations

3rdByte of Device Identifier Description

3rdcycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleaved Program Between Multiple die	Not Supported		0						
	Supported		1						
Cache Program	Not Supported	0							
	Supported	1							

Table 9 : Legacy Read ID 3rd byte description

4th Byte of Device Identifier Description

4th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (Without Spare Area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (Without Spare Area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Redundant Area Size (byte/512byte)	16						0		
	32						1		
Number of IO	x8		0						
	x16		1						
Serial Access Time(min)	45ns	0				0			
	25ns	1				0			
	Reserved	0				1			
	Reserved	1				1			

Table 10 : Legacy Read ID 4th byte description

5thByte of Device Identifier Description

5th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1bit/512Bytes 2bit/512Bytes 4bit/512Bytes 8bit/512Bytes							0 0 1 1	0 1 0 1
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size (W/O redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved		0							

Table 11 : Legacy Read ID 5th byte description

3.17. Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI" where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values.

3.18. Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters.
This data structure enables the host processor to automatically recognize the Nand Flash configuration of a device. The whole data structure is repeated at least three times.
The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.
The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.
Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

3.19.Parameter Page Data Structure Definition

For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data byte share in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

Byte	O/M	Description
		Revision information and features block
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page copy-back 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports copy-back 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command
10-31		Reserved (0)
		Manufacturer information block
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
		Memory organization block
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance

Byte	O/M	Description
		Memory organization block
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
		Electrical parameters block
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	t_{PROG} Maximum page program time (µs)
135-136	M	t_{BERS} Maximum block erase time (µs)
137-138	M	t_R Maximum page read time (µs)
139-140	M	tCCS Minimum change column setup time (ns)
141-163		Reserved (0)
		Vendor block
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
		Redundant Parameter Pages
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

4. Other Features

4.1. Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCCis below about 1.8 V (3.3 V Device) or 1.1 V (1.8 V Device). WP# pin provides hardware protection and is recommended to be kept at VILduring power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences. The two-step command sequence for program/erase provides additional software protection.

4.2. Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR(R/B#) and current drain during busy (Ibusy),Its value can be determined by the following guidance.

4.3 Write protect (#WP) handling

Erase and program operations are a aborted if WP# is driven low during busy time, and kept low for about 100nsec. Switching WP# low during this time is equivalent to issuing a Reset command (FFh)
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for tRST(similarly to Figure 23). At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the WP# value. Refer to Table 7 for more information on device status.
Erase and program operations are enabled or disabled by setting WP# to high or low respectively prior to issuing the setup commands (80h or 60h).
The level of WP# shall be set tWW nsec prior to raising the WE# pin for the set up command.

5.Device Parameters

5.1. Valid Blocks

	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	2008		2048	Blocks

Table 15 : Valid Blocks Number

Notes:
1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

5.2. Absolute Maximum Rating

Symbol	Parameter	Value	Unit
		Min	
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	℃
	Ambient Operating Temperature (Mobile Operating Temperature	-30 to 85	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	℃
V_{IO}	Input or Output Voltage	-0.6 to 4.6	V
V_{CC}	Supply Voltage	-0.6 to 4.6	V

Table 16 : Absolute maximum ratings

Notes:
1. Please contact to ATO Solution and confirm the availability of the product.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.
3. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
   Refer also to the ATO Solution Program and other relevant quality documents.

5.3. DC and Operating Characteristics(3.3v)

Parameter		Symbol	Test Condition	2.7V ~ 3.6V			Unit
				Min	Typ	Max	
Power on reset current		ICC0	FFh command input after power on	-	-	50 per device	mA
Operating current	Read	ICC1	tRC= tRC(min), CE#=VIL, IOUT=0㎃	-	15	30	mA
	Program	ICC2	Normal			30	mA
			Cache			40	mA
	Erase	ICC3	-		15	30	mA
Stand-by Current (TTL)		ICC4	CE#=VIH, WP#=0V/VCC			1	mA
Stand-by Current (CMOS)		ICC5	CE#=VCC-0.2, WP#=0V/VCC		10	50	uA
Input Leakage Current		ILI	VIN=0 to VCC(MAX)			±10	uA
Output Leakage Current		ILO	VOUT=0 to VCC(MAX)			±10	uA
Input High Voltage		VIH	-	Vccx0.8		Vcc+0.3	V
Input Low Voltage		VIL	-	-0.3		0.2xVcc	V
Output High Voltage Level		VOH	IOH=-400 ㎂	2.4			V
Output Low Voltage Level		VOL	IOL=2.1 ㎃			0.4	V
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.4V	8	10		mA

Table 17 : DC and Operating Characteristics

5.4. AC Test Conditions(3.3v)

Parameter	Value
	2.7V ≤ Vcc ≤ 3.6V
Input Pulse Levels	0 V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load(1.7V-1.95V)	1 TTL GATE and CL=50pF

Table 18 : AC Test Conditions

Note:
These parameters are verified device characterization and are not 100% tested.

5.5. DC and Operating Characteristics(1.8v)

Parameter		Symbol	Test Condition	1.7V ~ 1.95V			Unit
				Min	Typ	Max	
Power on reset current		ICC0	FFh command input after power on	-	-	50 per device	mA
Operating current	Read	ICC1	tRC= tRC(min), CE#=VIL, IOUT=0mA	-	10	20	mA
	Program	ICC2	Normal			20	mA
			Cache			30	mA
	Erase	ICC3	-		10	20	mA
Stand-by Current (TTL)		ICC4	CE#=VIH, WP#=0V/VCC			1	mA
Stand-by Current (CMOS)		ICC5	CE#=VCC-0.2, WP#=0V/VCC		10	50	uA
Input Leakage Current		ILI	VIN=0 to VCC(MAX)			±10	uA
Output Leakage Current		ILO	VOUT=0 to VCC(MAX)			±10	uA
Input High Voltage		VIH	-	Vccx0.8		Vcc+0.3	V
Input Low Voltage		VIL	-	-0.3		0.2xVcc	V
Output High Voltage Level		VOH	IOH=-100uA	VCC-0.1			V
Output Low Voltage Level		VOL	IOL=100uA			0.1	V
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.1V	3	4		mA

5.6. AC Test Conditions(1.8v)

Parameter	Value
	1.7V ≤ Vcc ≤ 1.95V
Input Pulse Levels	0 V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load(1.7V-1.95V)	1 TTL GATE and CL=30pF

Note:
These parameters are verified device characterization and are not 100% tested.

5.7. Pin Capacitance (TA=25℃, F=1.0㎒)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	10	pF
Input/Output Capacitance	CI/O	VI=0V	-	10	pF

5.8. Program/ Read / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	tPROG	-	300	700	us
Read Cache busy time	tCBSYR	-	5	tR	Us
Cache Program short busy time	tCBSYW	-	5	tPROG	us
Cache Program busy time(ONFI)	tPCBSY	-	5	tPROG	us
Multi-plane Erase busy time	tIEBSY	-	500	1000	ns
Multi-plane Program busy time(traditional)	tDBSY	-	500	1000	ns
Multi-plane Program busy time(ONFI)	tIPBSY	-	500	1000	ns
Number of Partial Program Cycles in the same page	NOP	-	-	4	cycles
Block Erase Time	tBERS	-	3.5	10	ms

Table 19 : Program / Erase Characteristics

Notes:
Typical value is measured at Vcc=3.3V, TA=25℃(3.3V Device) or Vcc=1.8 V, TA=25℃ (1.8V Device). .
Not 100% tested.

5.9. AC Timing Characteristics

Parameter	Symbol	3.3V		1.8V		Unit
		Min	Max	Min	Max	
CLE setup Time	tCLS	12	-	25	-	ns
CLE Hold Time	tCLH	5	-	10	-	ns
/CE setup Time	tCS	20	-	35	-	ns
/CE Hold Time	tCH	5	-	10	-	ns
/WE Pulse Width	tWP	12	-	25	-	ns
ALE setup Time	tALS	12	-	25	-	ns
ALE Hold Time	tALH	5	-	10	-	ns
Data setup Time	tDS	12	-	20	-	ns
Data Hold Time	tDH	5	-	10	-	ns
Write Cycle Time	tWC	25	-	45	-	ns
/WE High Hold Time	tWH	10	-	15	-	ns
Address to Data loading Time	tADL	70	-	100	-	ns
Data Transfer from Cell to Register	tR	-	30	-	30	us
ALE to /RE Delay	tAR	10	-	10	-	ns
CLE to /RE Delay	tCLR	10	-	10	-	ns
Ready to /RE Low	tRR	20	-	20	-	ns
/RE Pulse Width	tRP	12	-	25	-	ns
WE High to Busy	tWB	-	100	-	100	ns
Read Cycle Time	tRC	25	-	45	-	ns
/RE Access Time	tREA	-	20	-	30	ns
/RE High to Output Hi-Z	tRHZ	-	100	-	100	ns
/CE High to Output Hi-Z	tCHZ	-	30	-	50	ns
/CE High to ALE or CLE Don't Care	tCSD	10	-	10	-	ns
/RE high to Output Hold	tRHOH	15	-	15	-	ns
/RE Low to Output Hold	tRLOH	5	-	-	-	ns
/RE or /CE High to Output hold	tCOH	15	-	15	-	ns
/RE High Hold Time	tREH	10	-	15	-	ns
Output Hi-Z to /RE Low	tIR	0	-	0	-	ns
/RE High to /WE Low	tRHW	100	-	100	-	ns
/WE High to /RE Low	tWHR	60	-	60	-	ns
CE# low to RE# low	tCR	10	-	10	-	Ns
Device resetting time (Read/Program/Erase)	tRST	-	5/10/500	-	5/10/500	us
Write protect time	tWW	100		100	-	ns

Table 20 : AC Timing Characteristics

Notes:
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

6. Timing Diagrams

Command Latch Cycle Timings

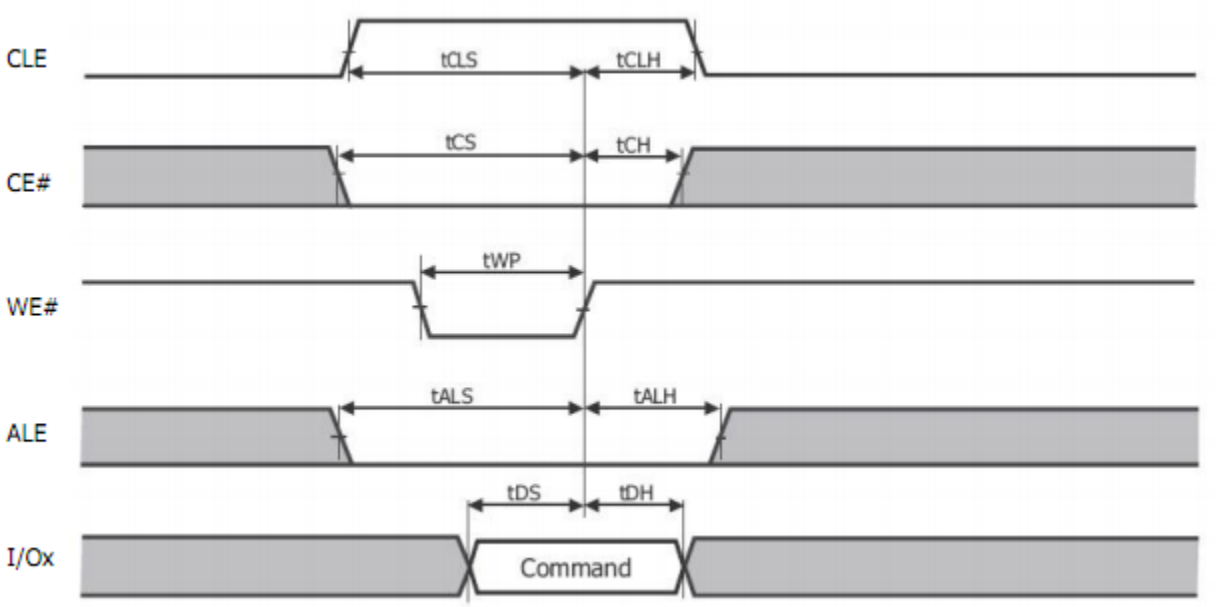


Figure 6 : Command latch timings

Address Latch Cycle Timings

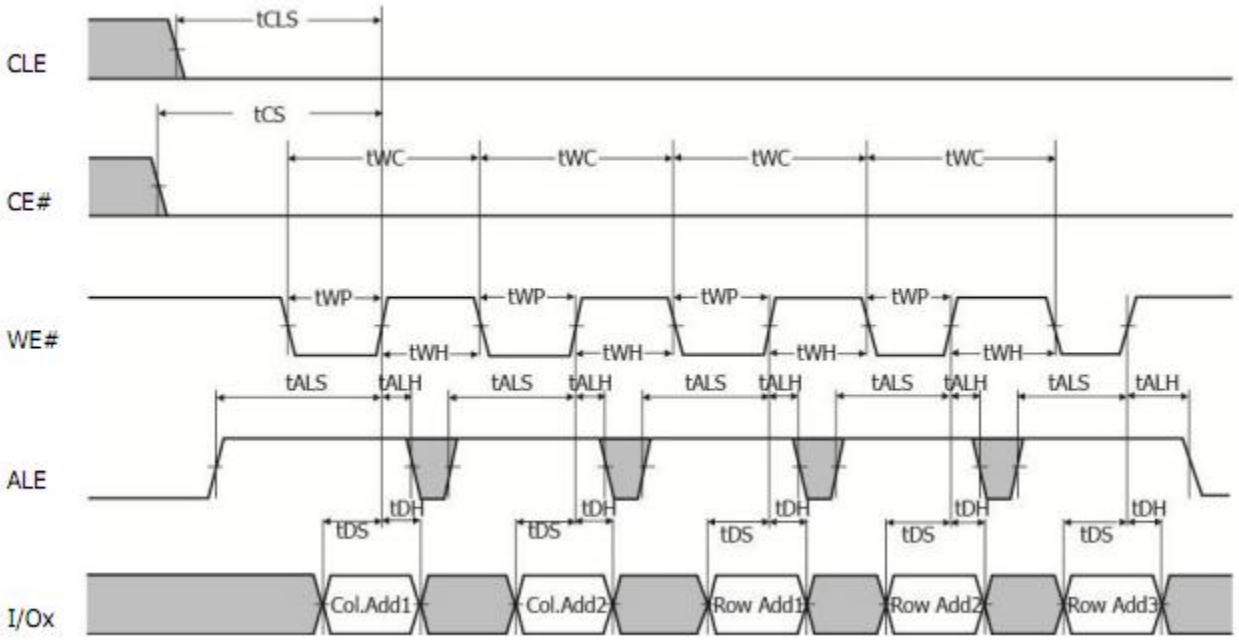


Figure 7 : Address latch timings

Data Input Cycle Timings

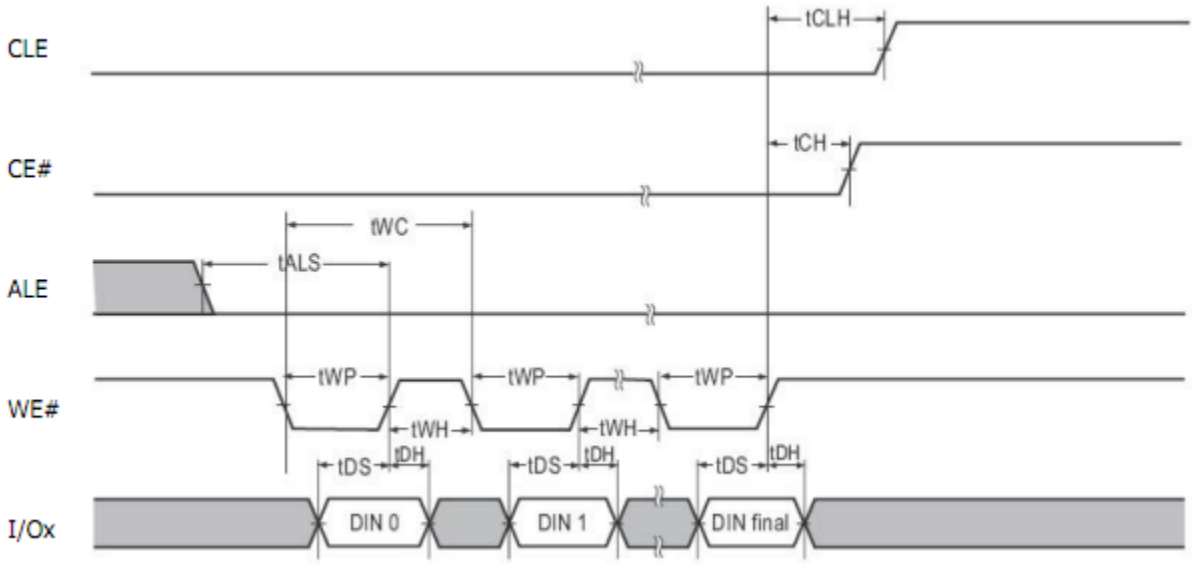


Figure 8 : Data Input cycle timings

Note:
Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

Data Output Cycle Timings (CLE=L, WE#=H, ALE=L, WP#=H)

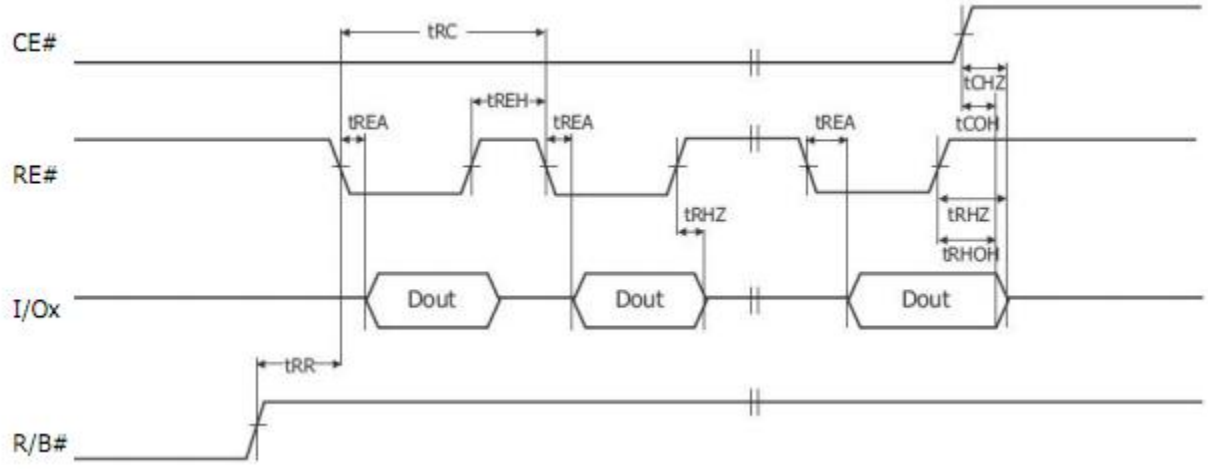


Figure 9 : Data output cycle timings

Notes:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRHOH is valid when frequency is lower than 33 MHz.

Data Output Cycle Timings (EDO type, CLE=L, WE#=H, ALE=L)

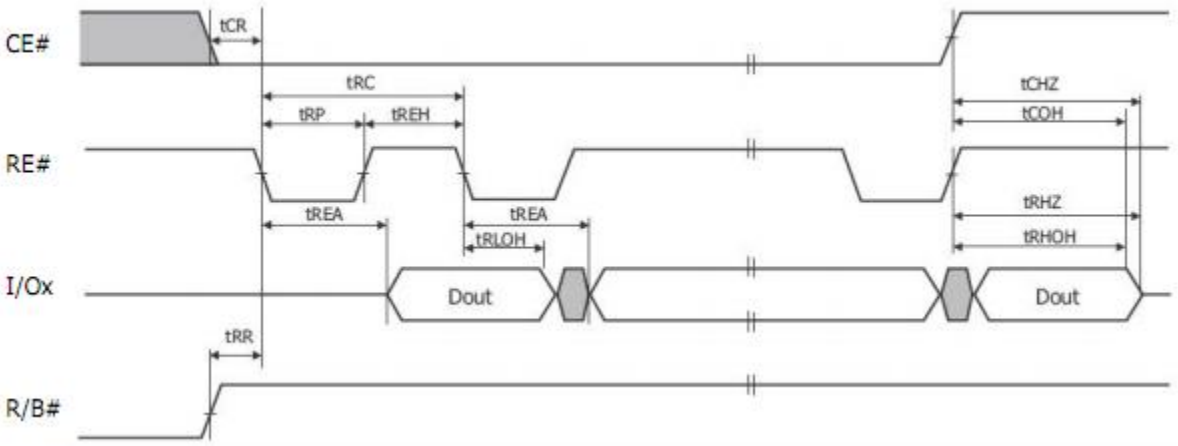


Figure 10 : Data output cycle timings (EDO)

Notes:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRLOH is valid when frequency is higher than 33 MHz. tRHOH starts to be valid when frequency is lower than 33 MHz.

Read Status Cycle Timings

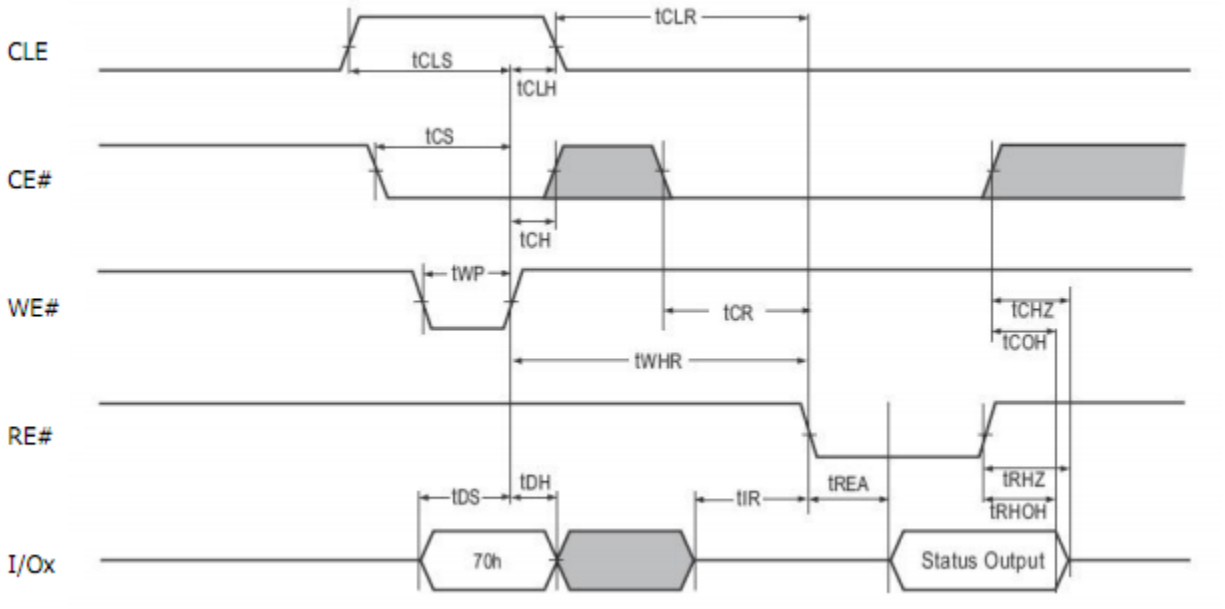


Figure 11A : Read status timings

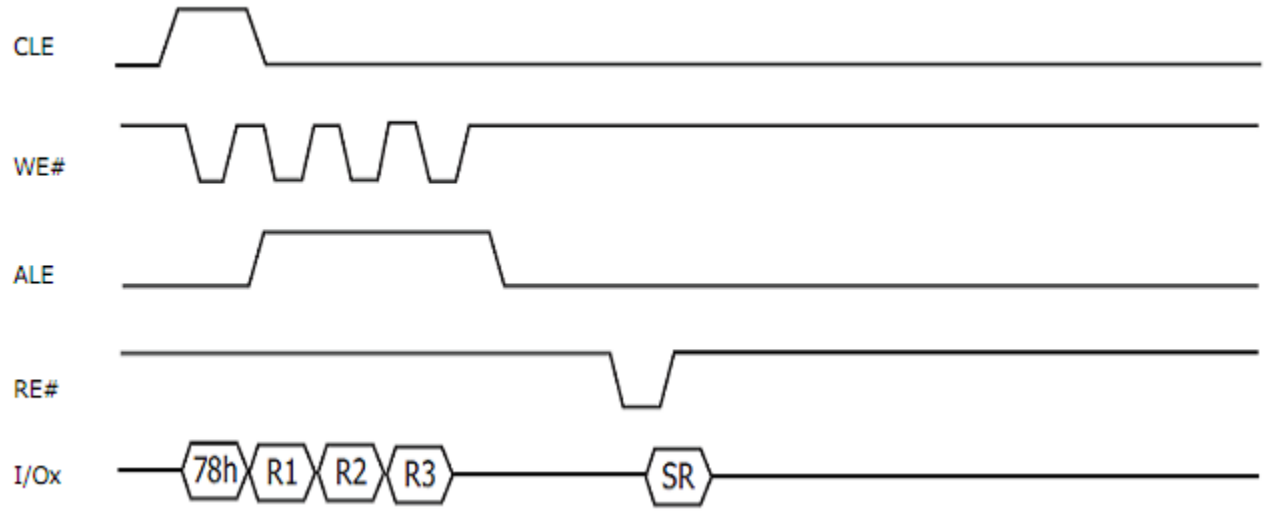


Figure 11B : Read Status Enhanced cycle

Page Read Operation Timings (Intercepted by CE#)

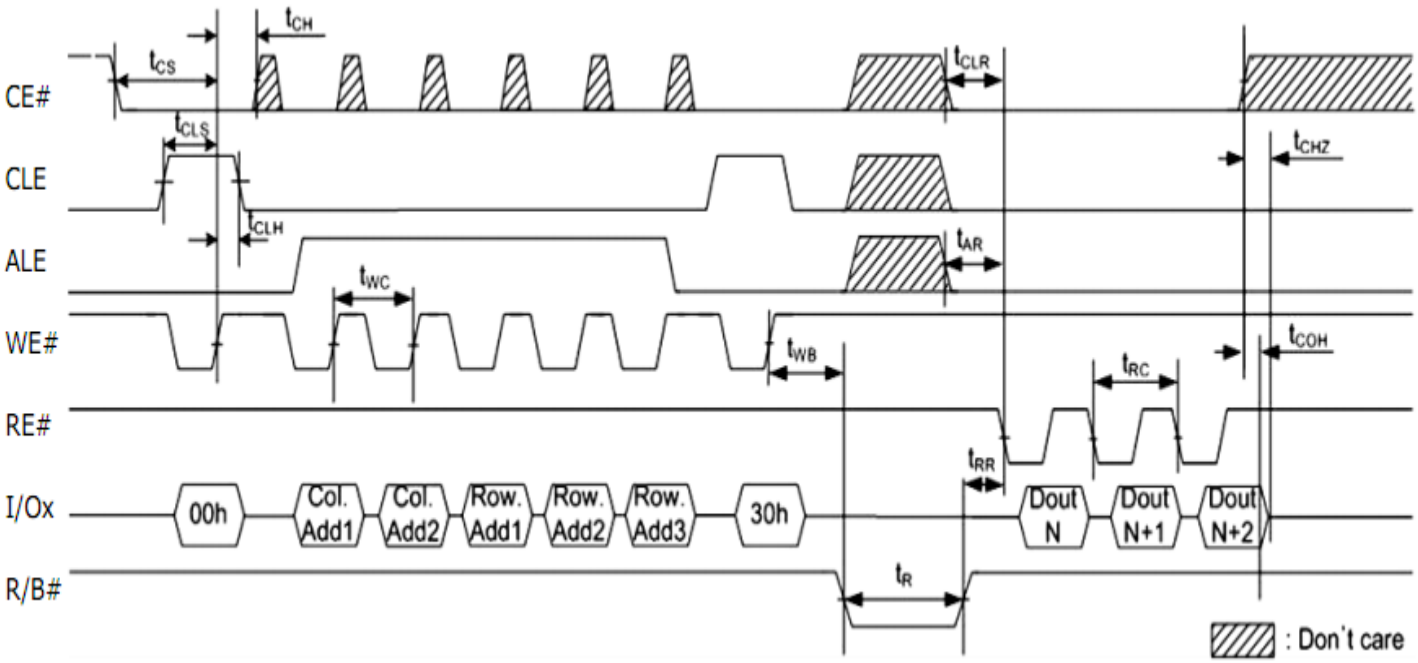


Figure 12 : Page read operation Timings (Intercepted by CE#)

Page Read Operation Timings with CE# don't care

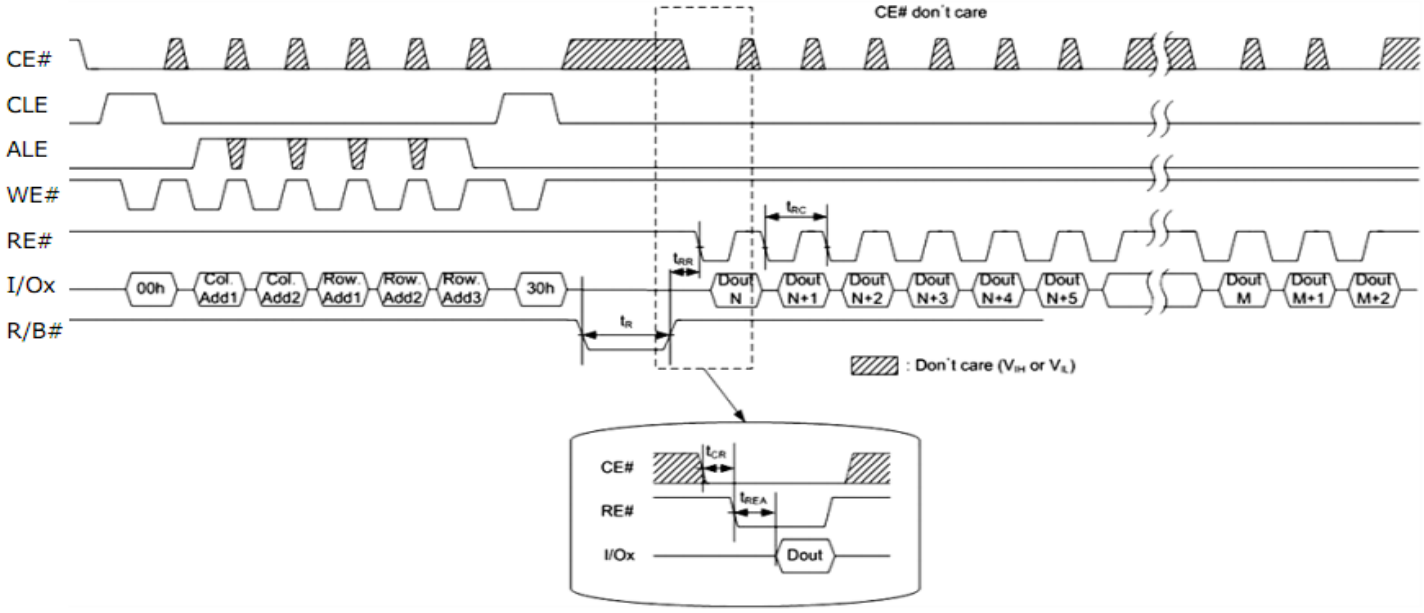


Figure 13 : Page Read Operation Timings with CE# don't care

Random Data Output Timings

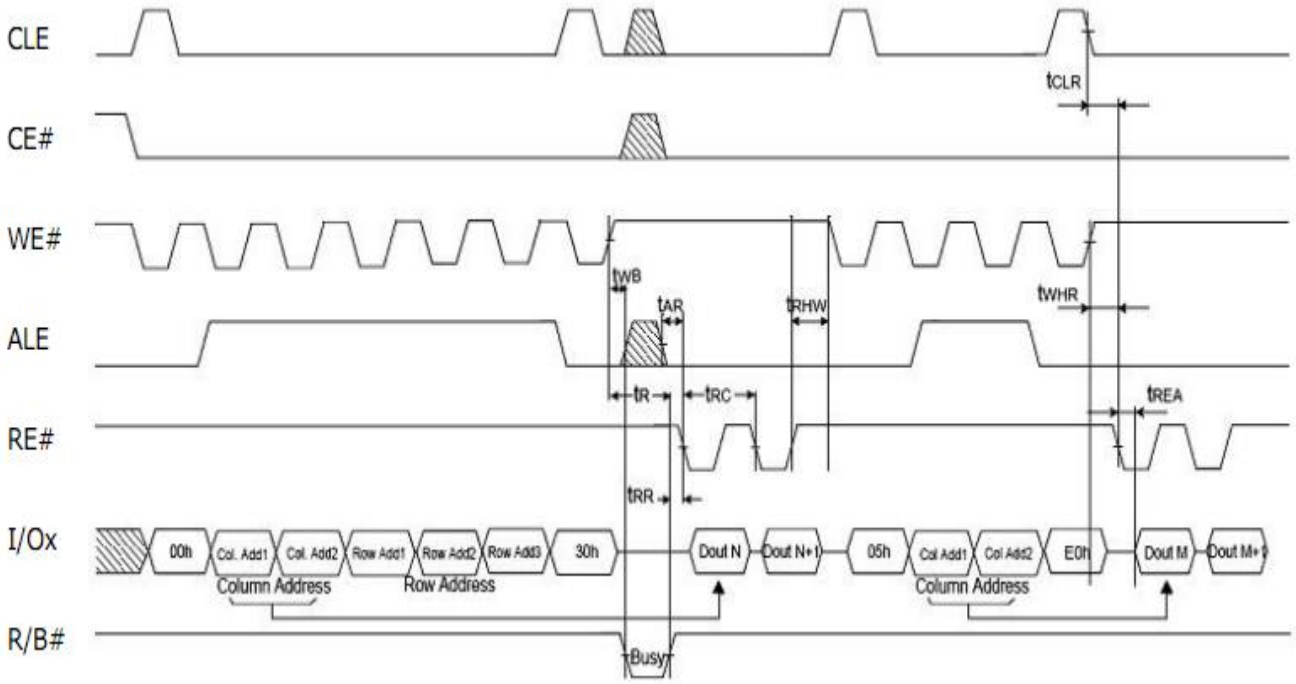


Figure 14 : Random data output timings

Cache Read Operation Timings

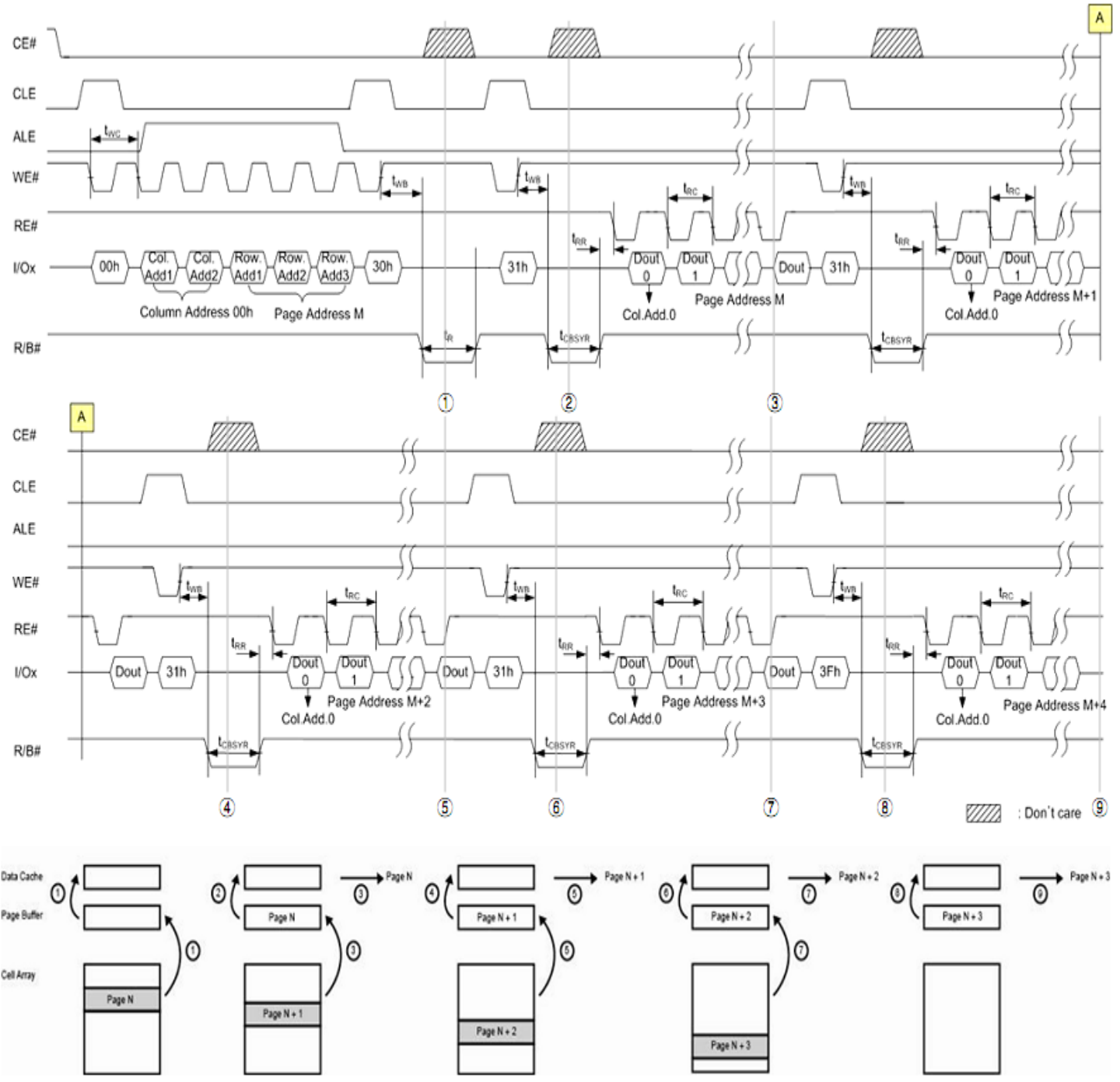


Figure 15 : Cache Read Operation Timings

Read ID Operation Timings

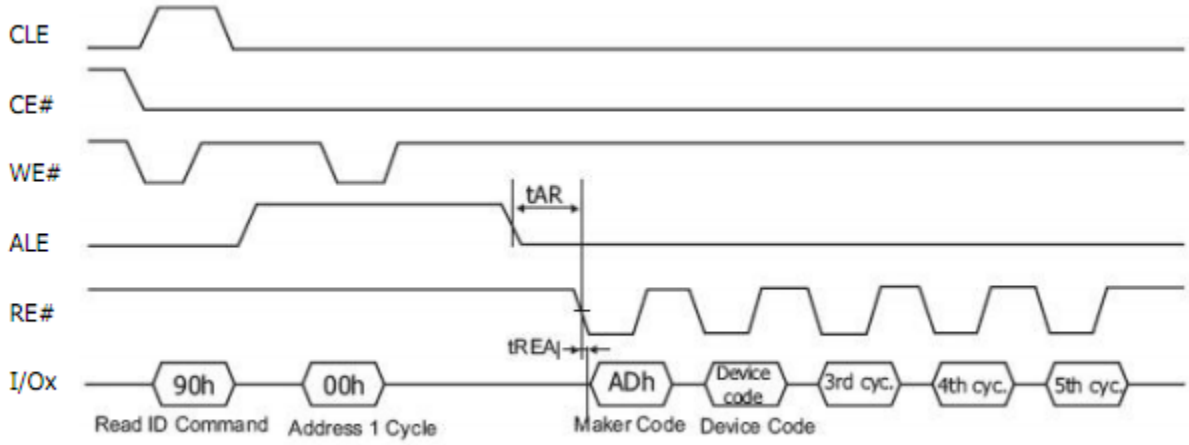


Figure 16 : Read ID operation timings

Page Program Operation Timings

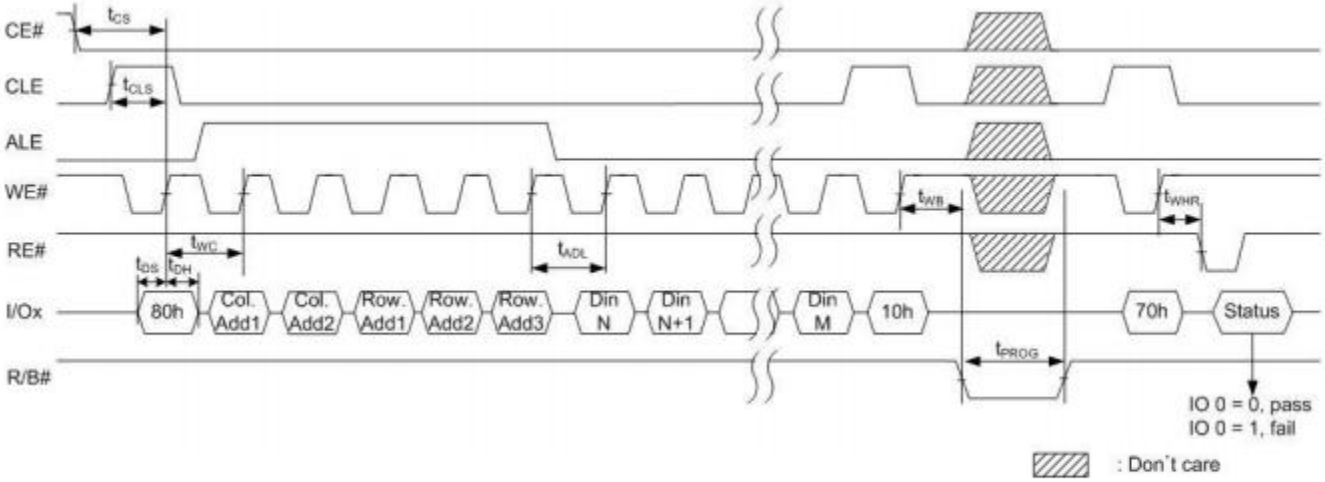


Figure 17 : Page Program Operation Timings

Note:
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Page Program Operation Timings with CE# don't care

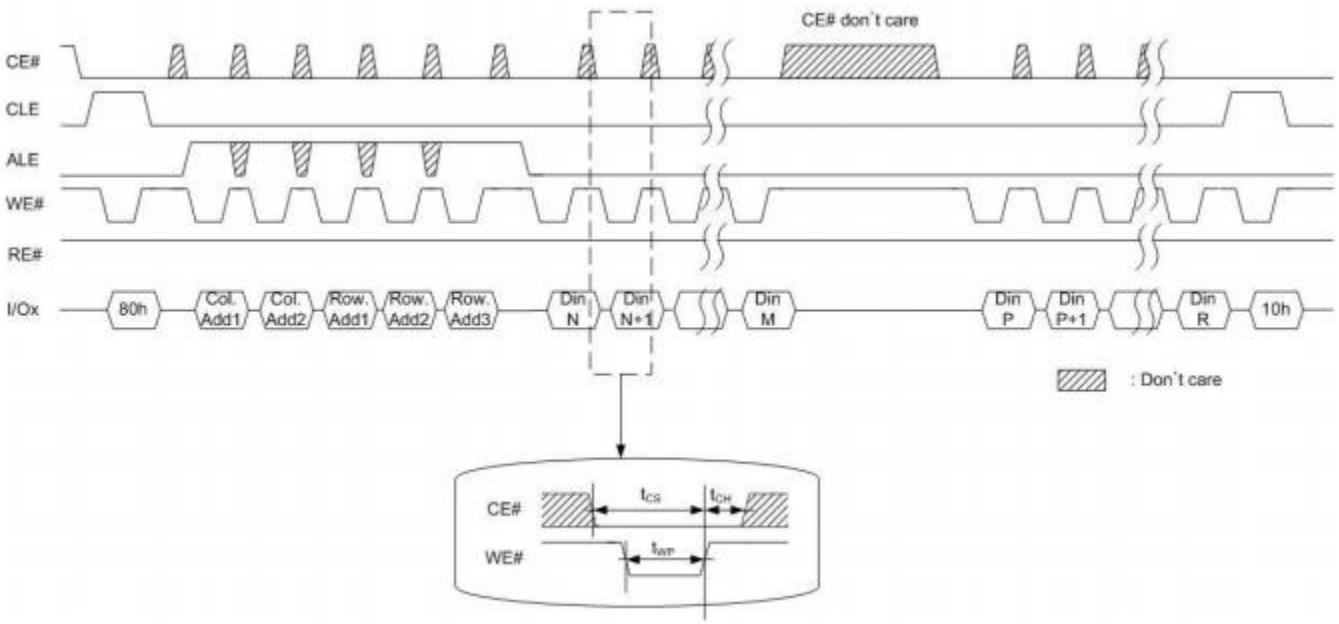


Figure 18 : Page program operation timings with CE# don't care

Note:
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Random Data Input Timings

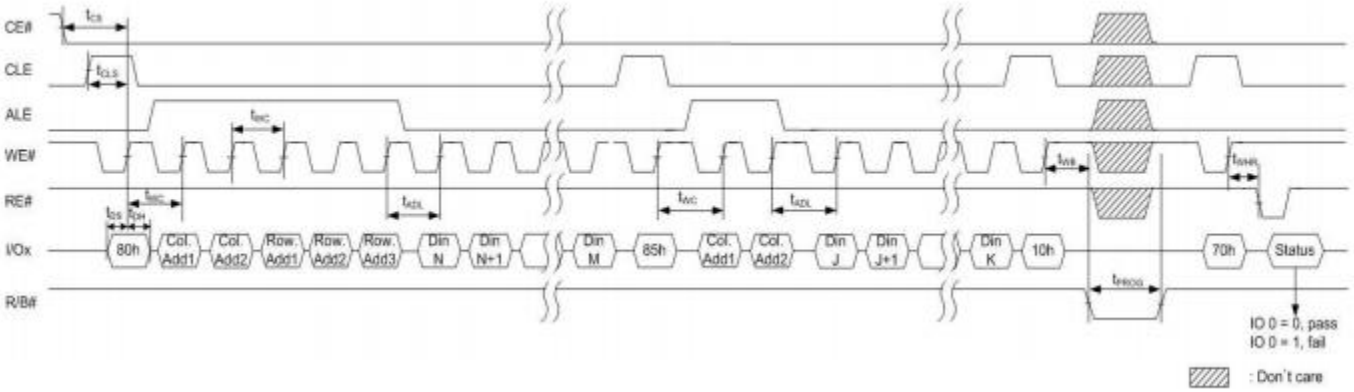


Figure 19 : Random Data Input Timings

Notes:
1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
2. Random data input can be performed in a page.

Copy-Back Program Operation Timings with Random Data Input

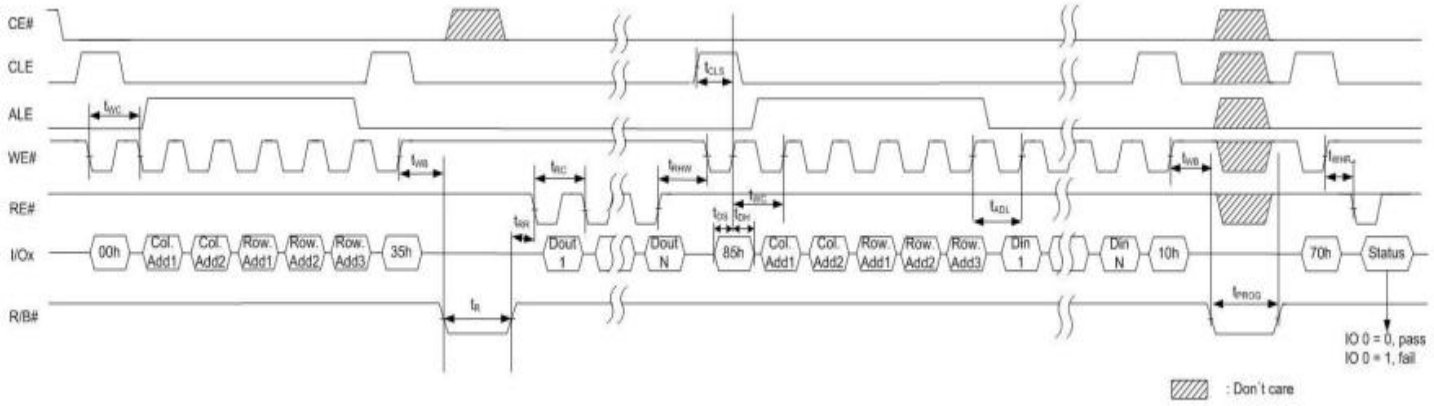


Figure 20 : Copy-back program operation timing with random data input

Notes:

1. Copy-Back Program operation is allowed only within the same memory plane.
2. On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Cache Program Operation Timings

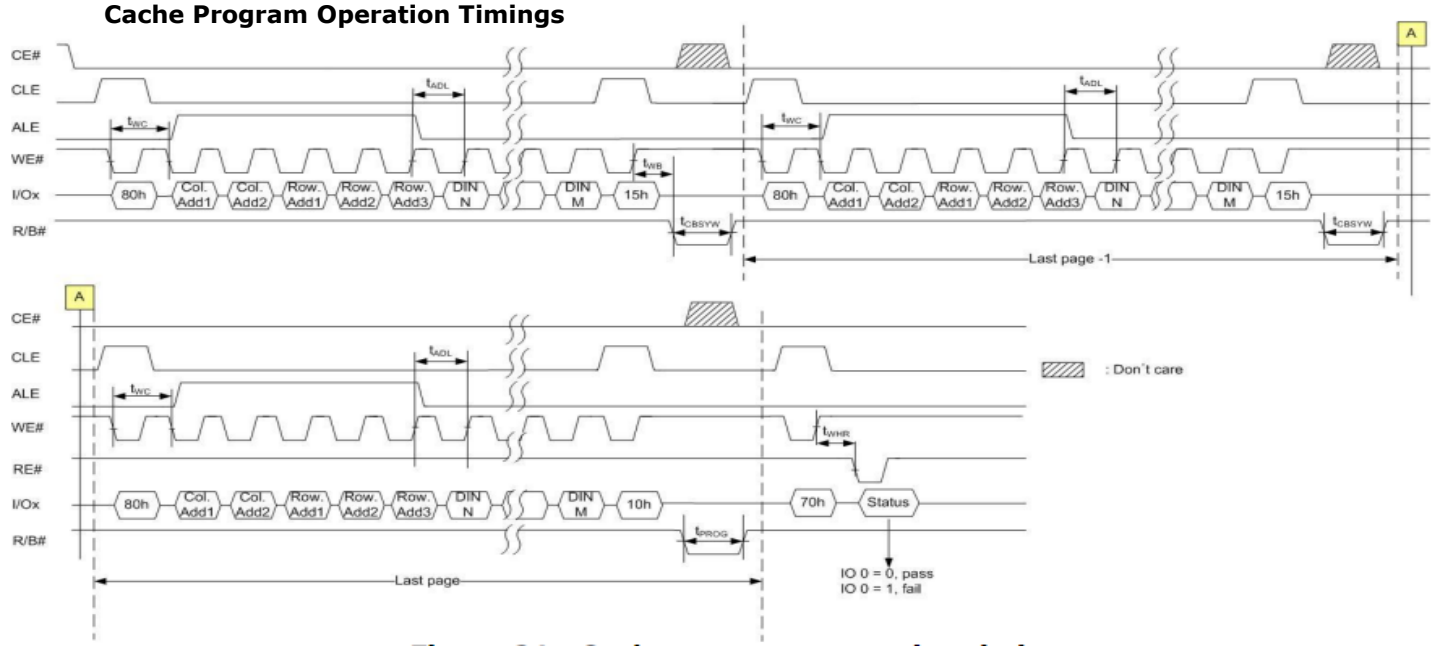


Figure 21 : Cache program operation timings

Note:

tPROG = Program time for the last page + Program time for the (last -1)th page
- (command input cycle time + address input cycle time + Last page data loading time)

Block Erase Operation Timings

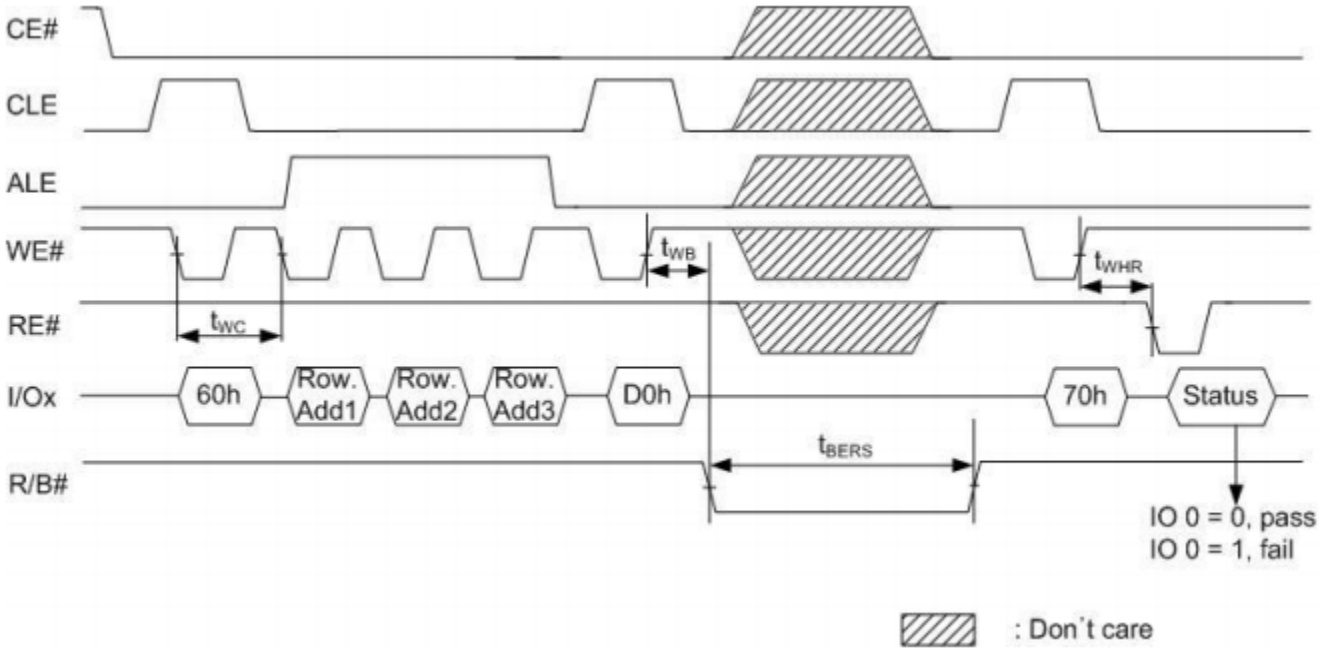


Figure 22 : Block erase operation timings

Reset Timings

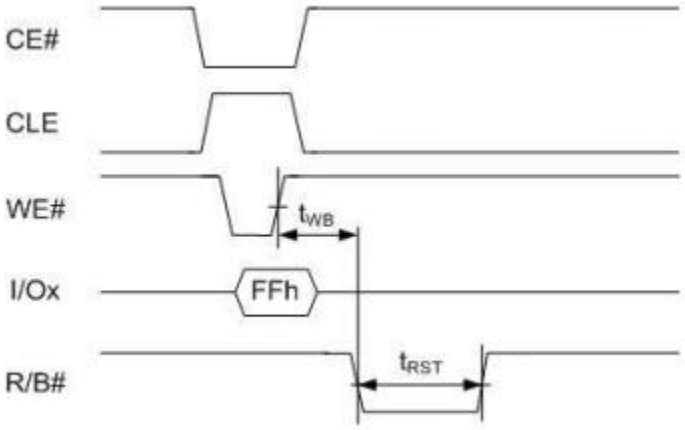


Figure 23 : Reset timings

Multi-plane program

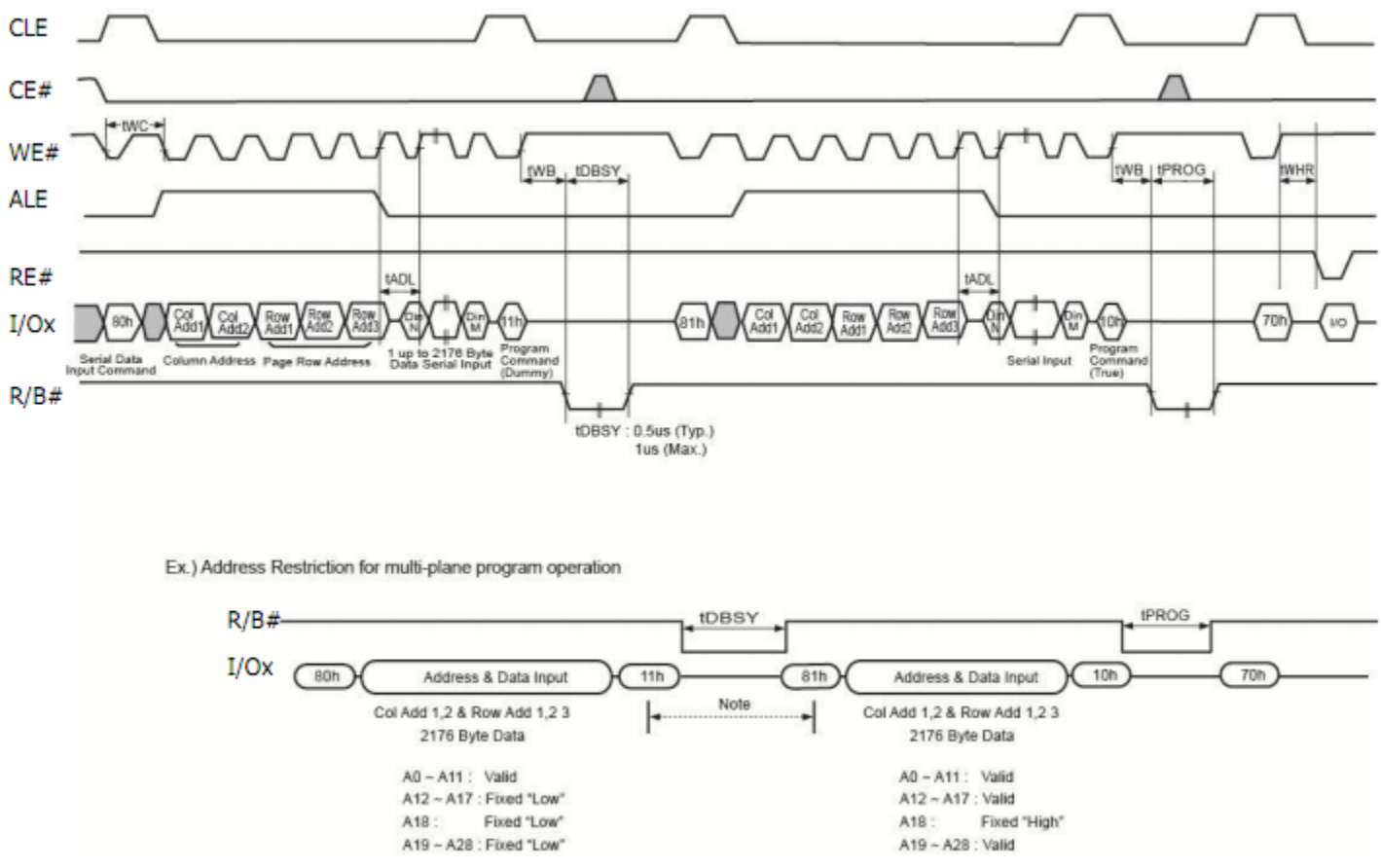


Figure 24 : Multi-plane page program (traditional protocol)

Notes:
1. The figure refers to x8 case. Please refer to Section 1.4 for address remapping rules for the x16 case
2. Any command between 11h and 81h is prohibited except 70h, 78h and FFh

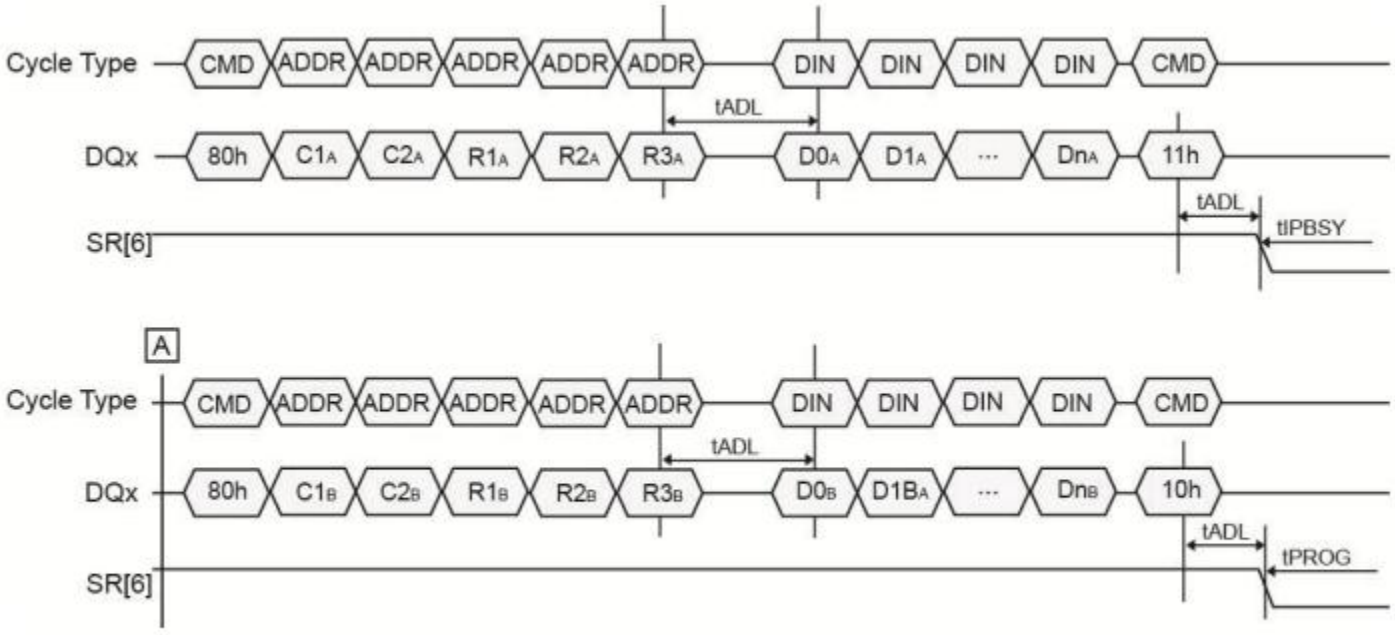
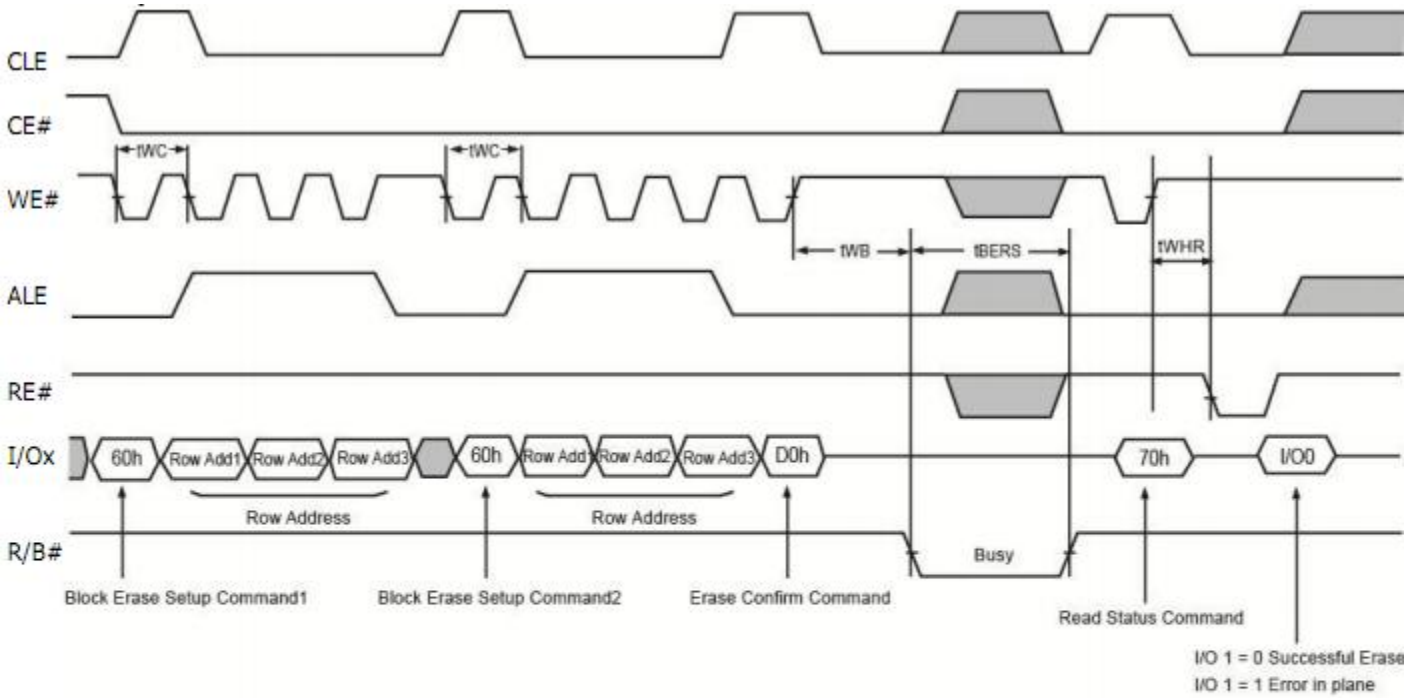


Figure 25 : Multi-plane page program (ONFI 1.0 protocol)

Notes:
C1A-C2A Column address for page A. C1A is the least significant byte.
R1A-R3A Row address for page A. R1A is the least significant byte.
D0A-DnA Data to program for page A.
C1B-C2B Column address for page B. C1B is the least significant byte.
R1B-R3B Row address for page B. R1B is the least significant byte.
D0B-DnB Data to program for page B.

Same restrictions on address of pages A and B, and allowed commands as **Figure 24** apply

Multi-plane Block Erase



Ex.) Address Restriction for Two-Plane Block Erase Operation

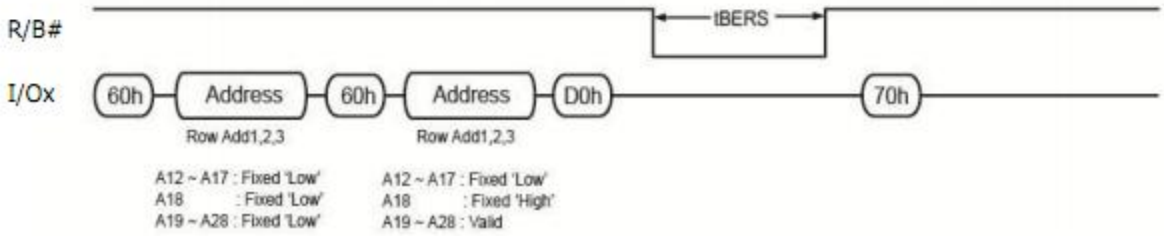


Figure 26 : Multi-plane block erase (traditional protocol)

Note:
The figure refers to x8 case. Please refer to Section 1.7 for address remapping rules for the x16 case

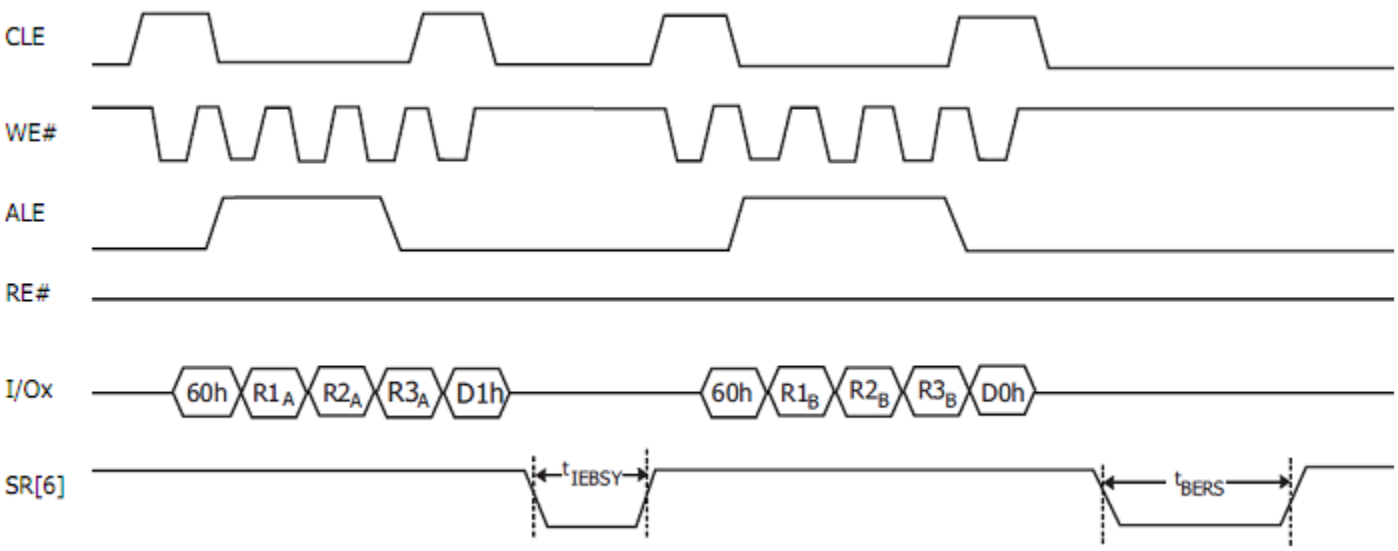


Figure 27 : Multi-plane block erase (ONFI 1.0 protocol)

Notes:
R1A-R3A Row address for block on plane 0. R1A is the least significant byte.
R1B-R3B Row address for block on plane 1. R1B is the least significant byte.
Same restrictions on address of blocks on plane 0(A) and 1(B) and allowed commands as Figure 30 apply

Multi-plane copy-back Program

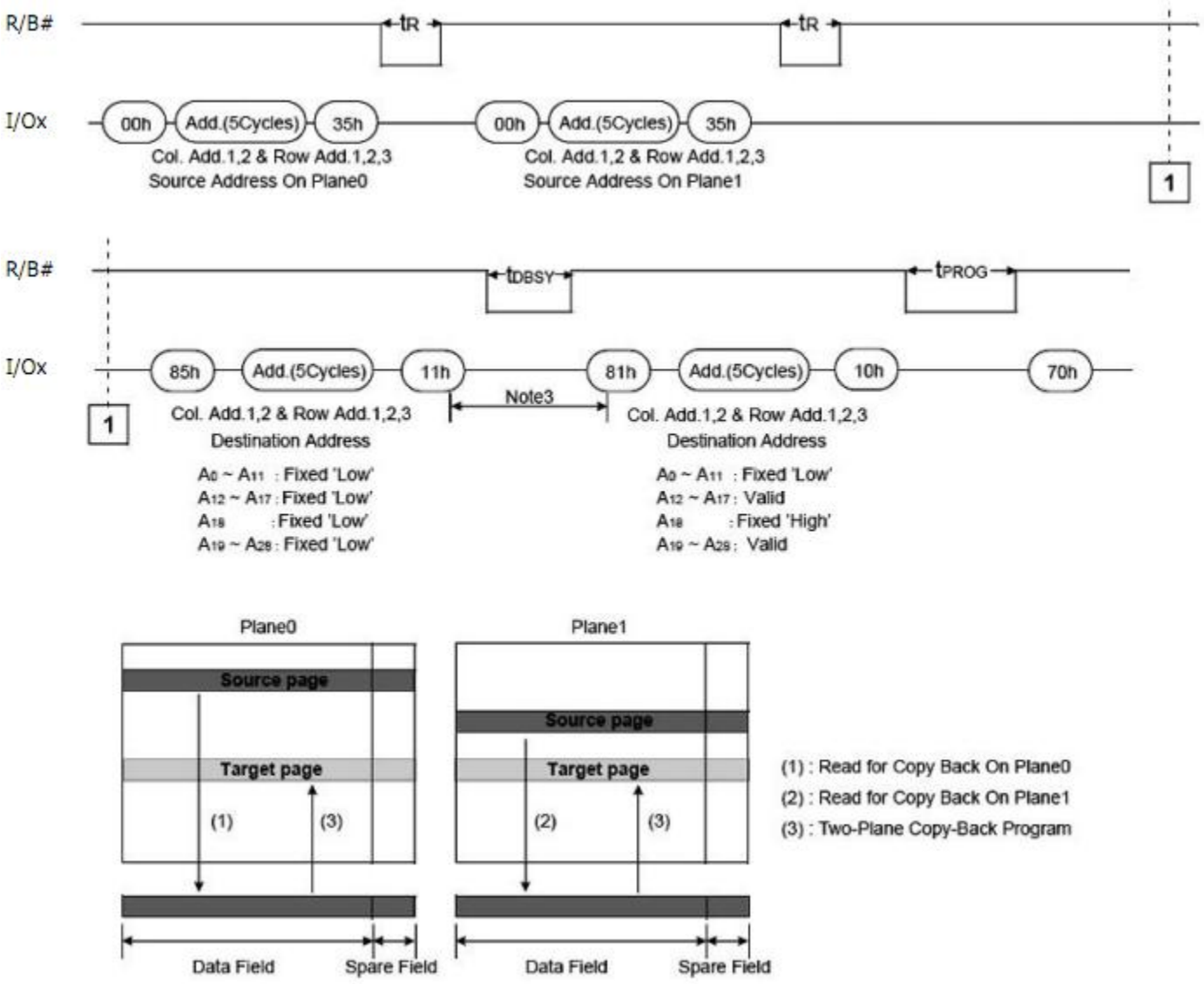


Figure 28 : Multi-plane copy-back program (traditional protocol)

Notes:
1. Copy-back program operation is allowed only within the same memory plane
2. On the same plane it is prohibited to operate copy-back program from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page).
Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. Any command between 11h and 81 h is prohibited except 70h and FFh.
4. The figure refers to x8 case. Please refer to **Section 1.7** for address remapping rules for the x16 case.

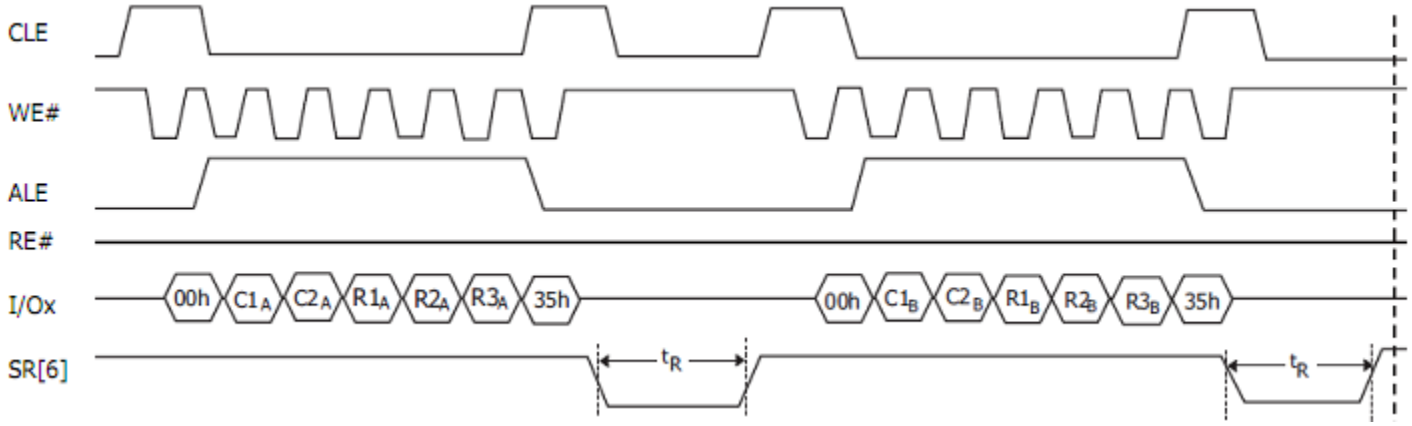


Figure 29 : Multi-plane copy-back read (ONFI 1.0 protocol)

Notes:
C1A-C2A Column address for page A. C1A is the least significant byte.
R1A-R3A Row address for page A. R1A is the least significant byte.
C1B-C2B Column address for page B. C1B is the least significant byte.
R1B-R3B Row address for page B. R1B is the least significant byte.

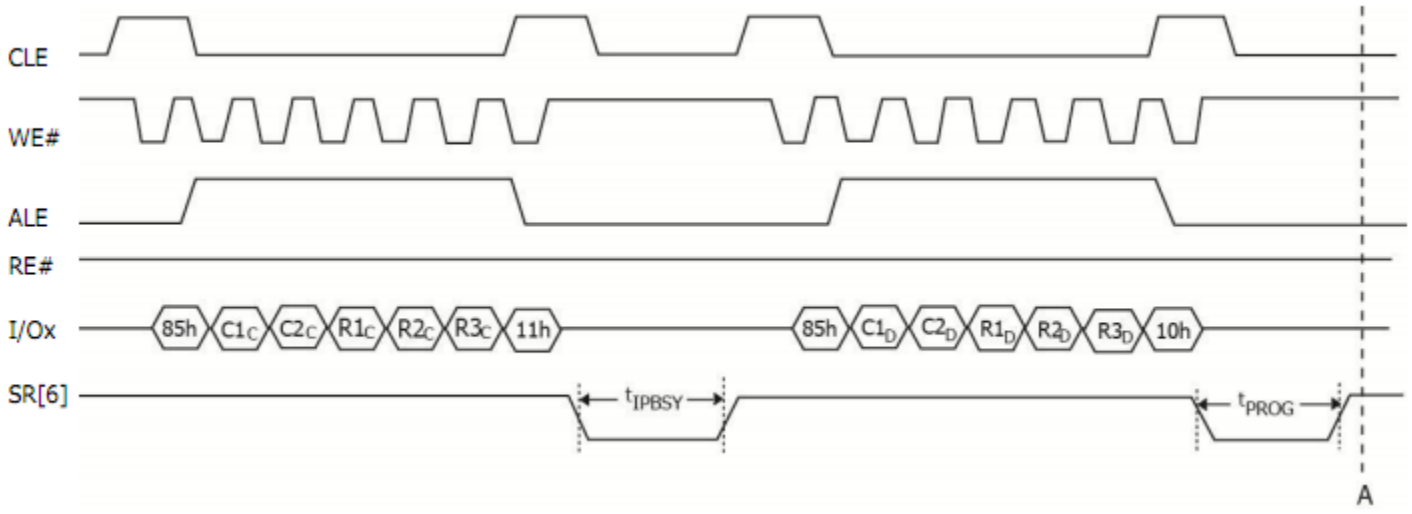


Figure 30 : Multi-plane copy-back program (ONFI 1.0 protocol)

Notes:
C1C-C2C Column address for page C. C1A is the least significant byte.
R1C-R3C Row address for page C. R1A is the least significant byte.
D0C-DnC Data to program for page C.
C1D-C2D Column address for page D. C1B is the least significant byte.
R1D-R3D Row address for page D. R1B is the least significant byte.
D0D-DnD Data to program for page D.

Same restrictions on address of pages C and D, and allowed commands as Figure 28 apply

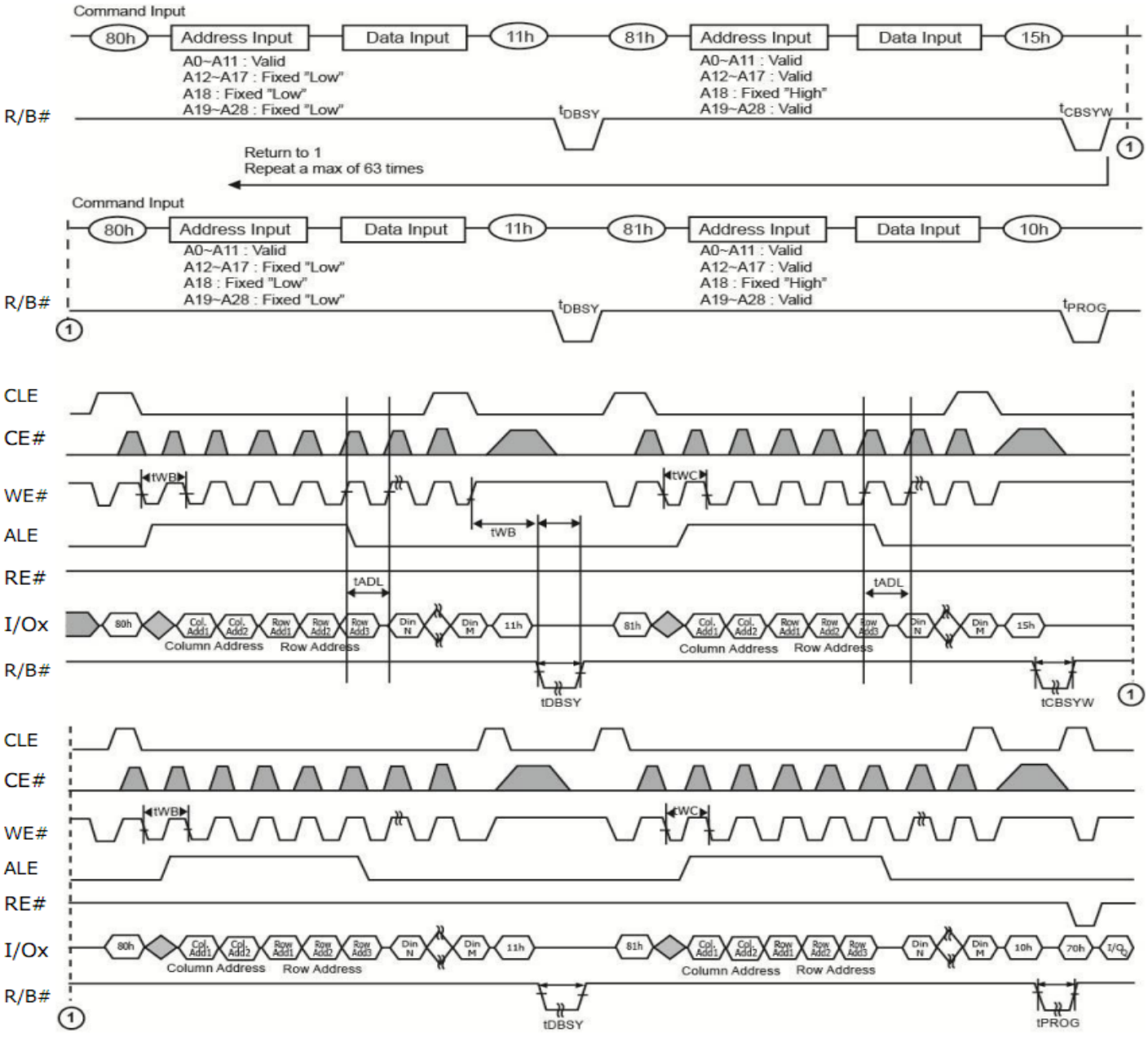


Figure 31 : Multi-plane cache program (traditional protocol)

Notes:
1. The figure refers to x8 case. Please refer to Section 1.7 for address remapping rules for the x16 case.
2. Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

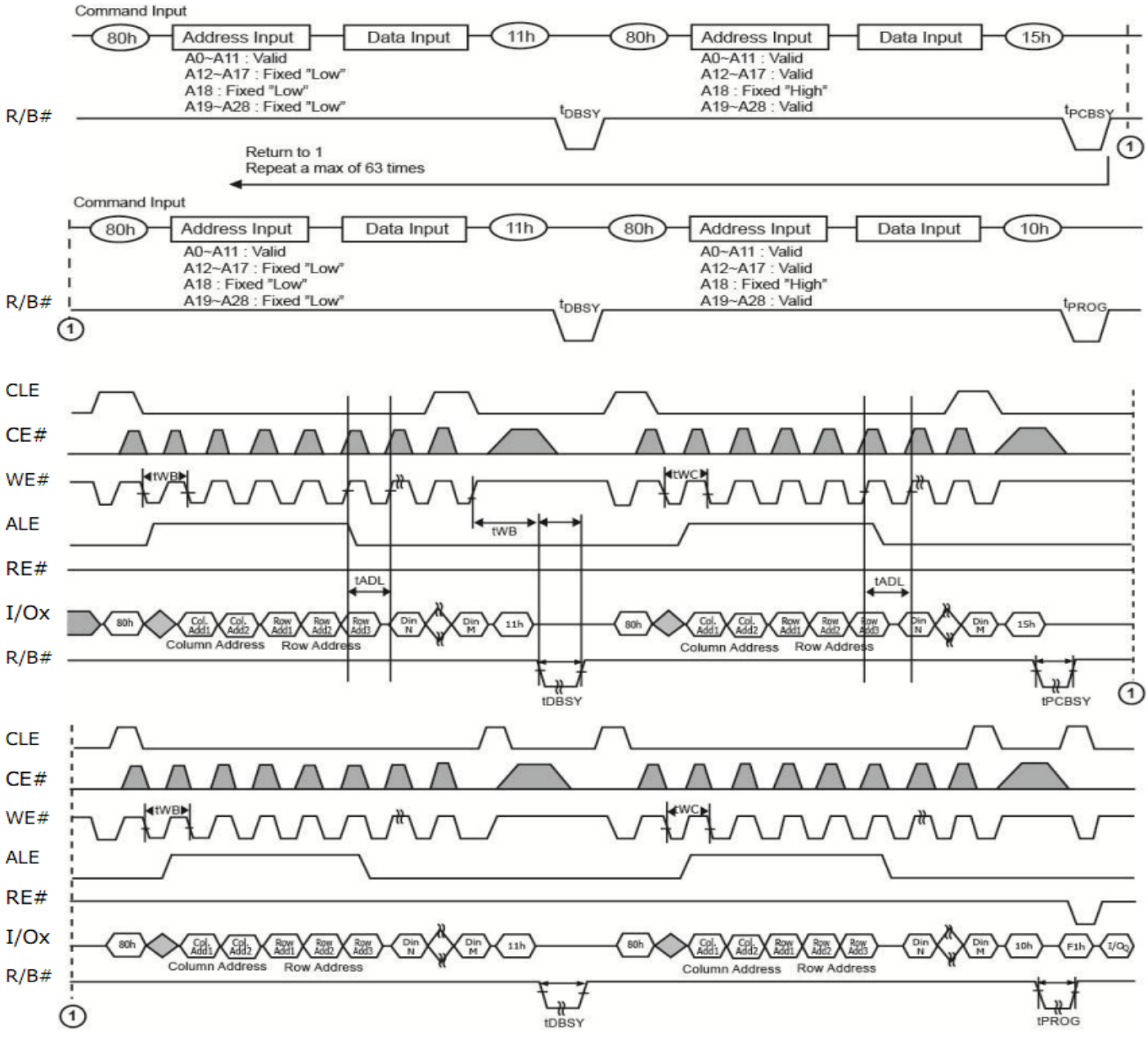


Figure 32 : Multi-plane cache program (ONFI protocol)

Notes:
1. The figure refers to x8 case. Please refer to Section 1.7 for address remapping rules for the x16 case.
2. Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

Page Re-program

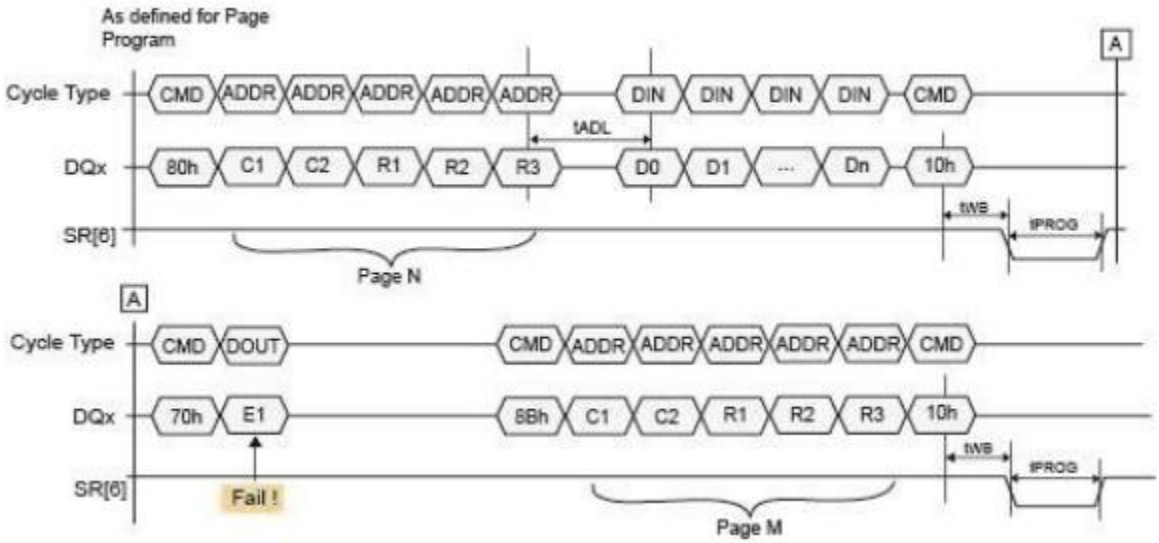


Figure 33 : Page Re-program

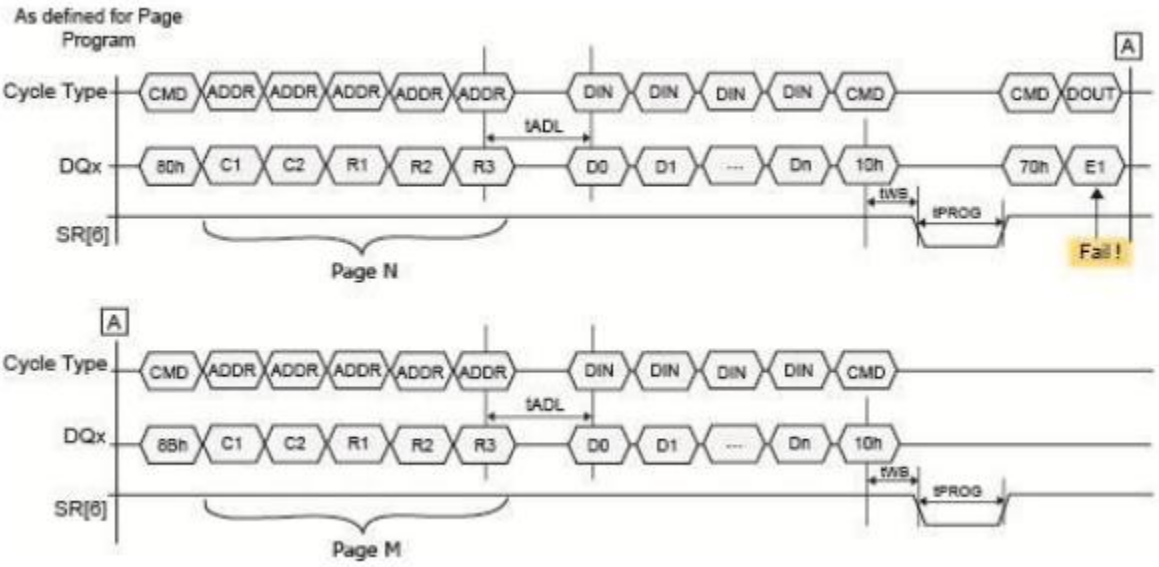


Figure 34 : Page Re-program with data manipulation

Multi-plane Page Re-program

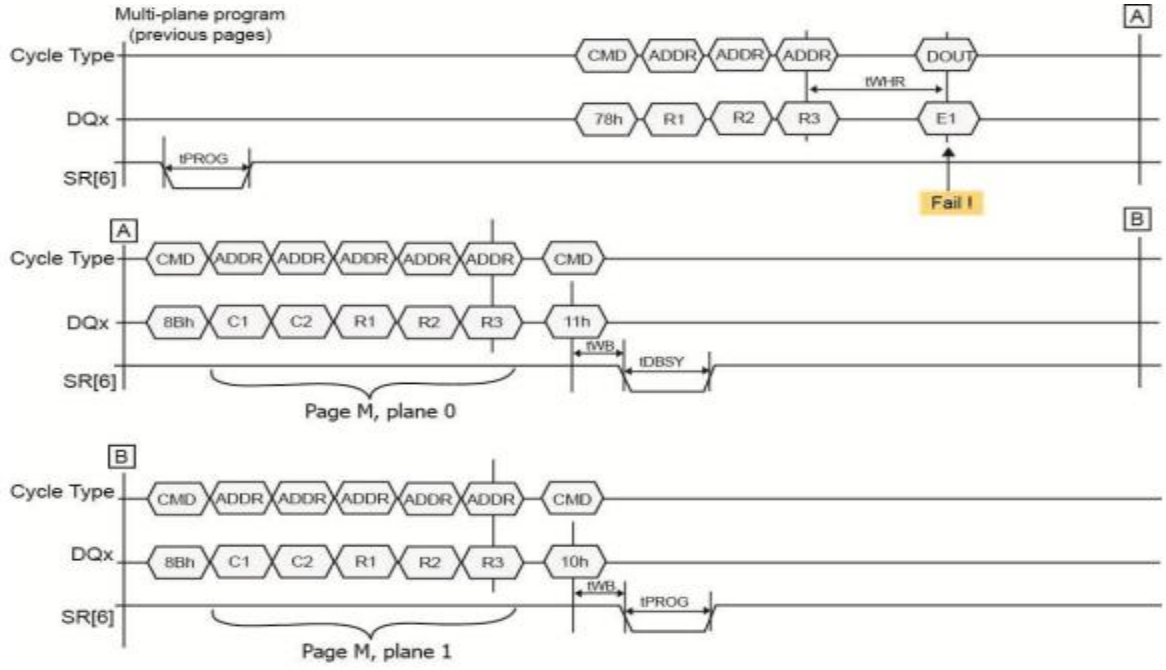


Figure 35 : Multi-plane Page Re-program

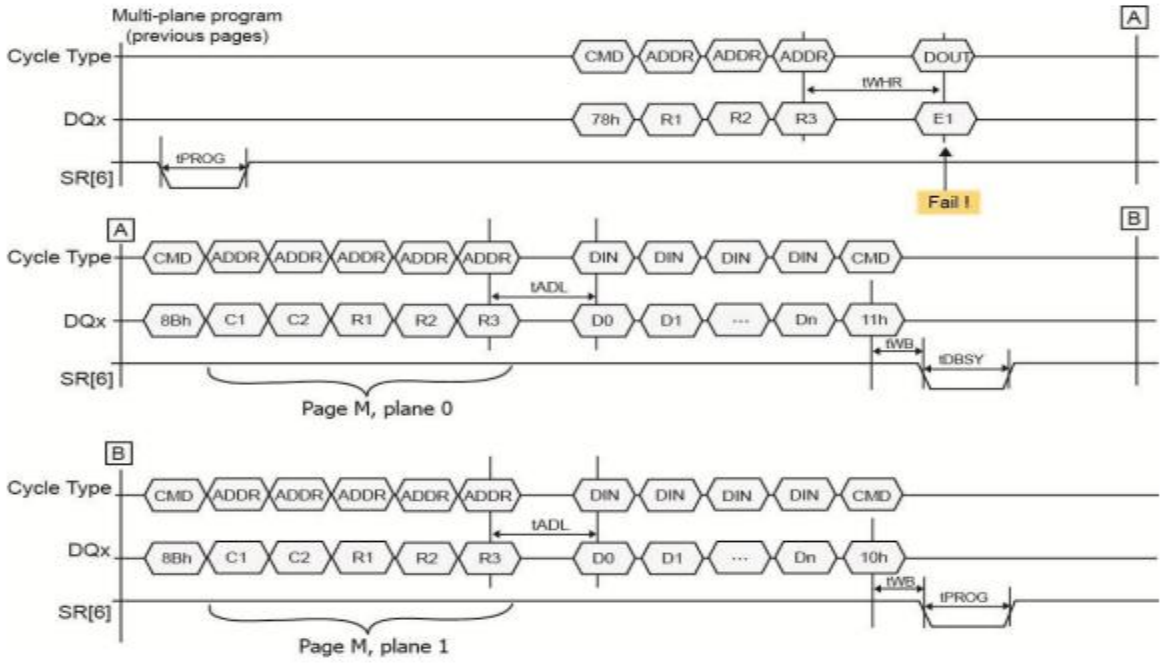


Figure 36 : Multi-plane Page Re-program with data manipulation

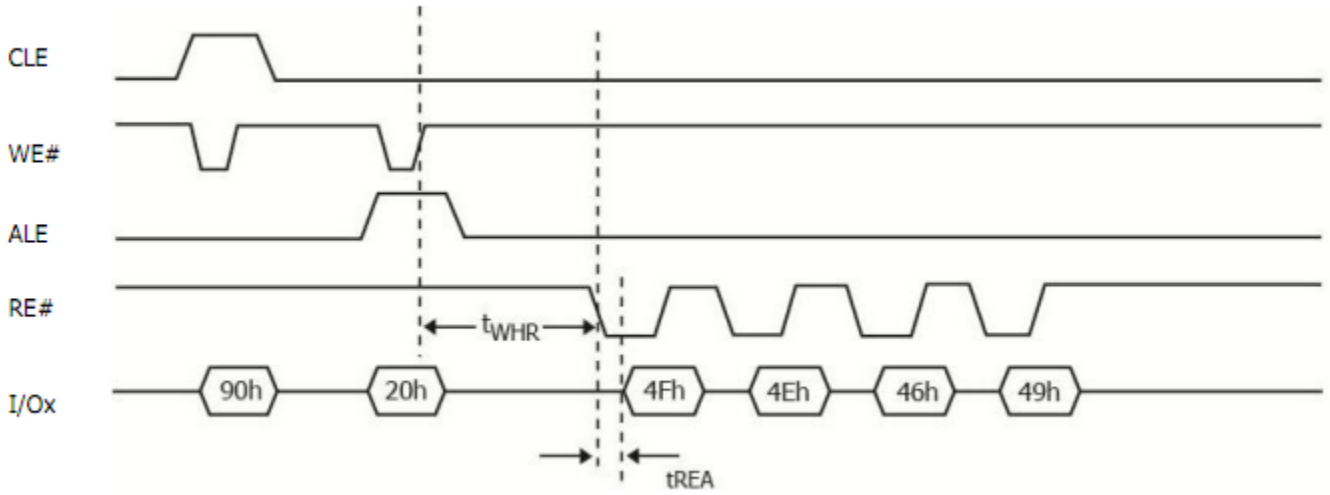


Figure 37 : ONFI signature timing

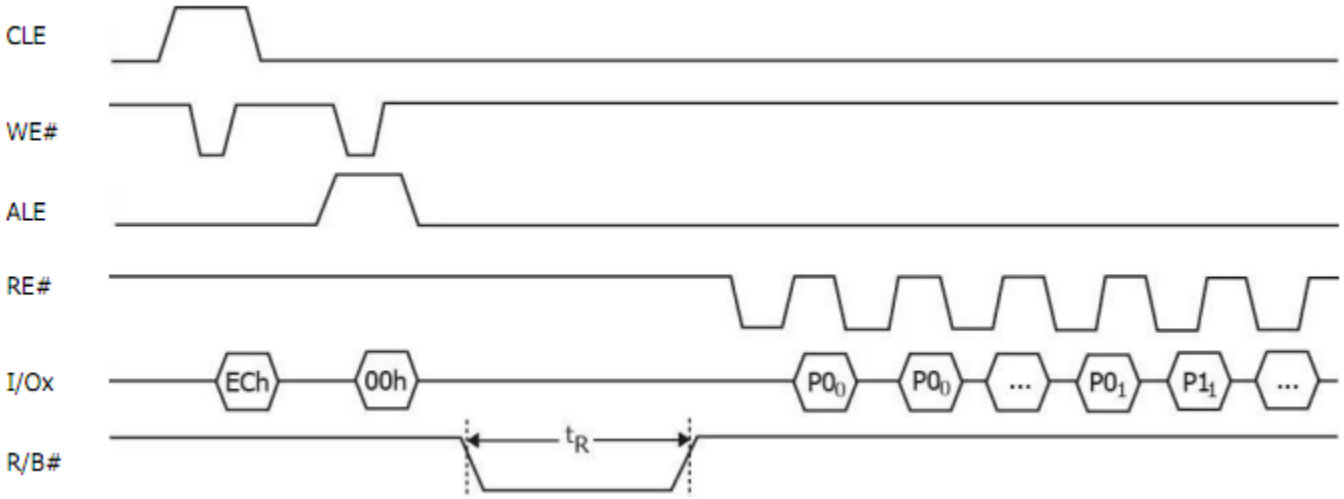


Figure 38 : Read Parameter Page timings

Data Protection & Power on/off Sequence

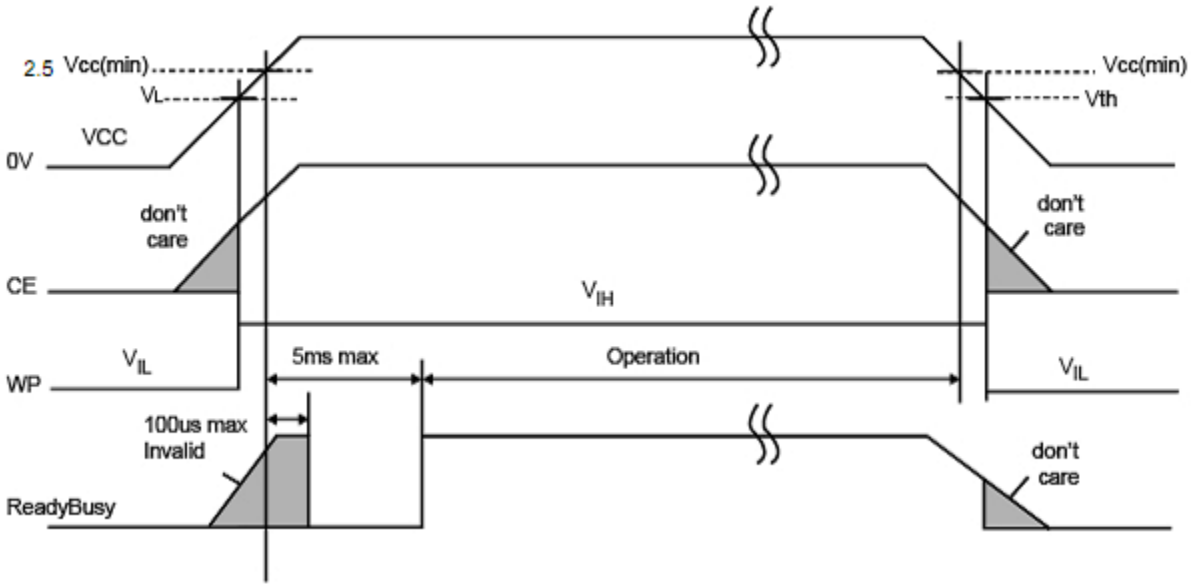


Figure 39 : Data protection and Power on/off(3.3V Device)

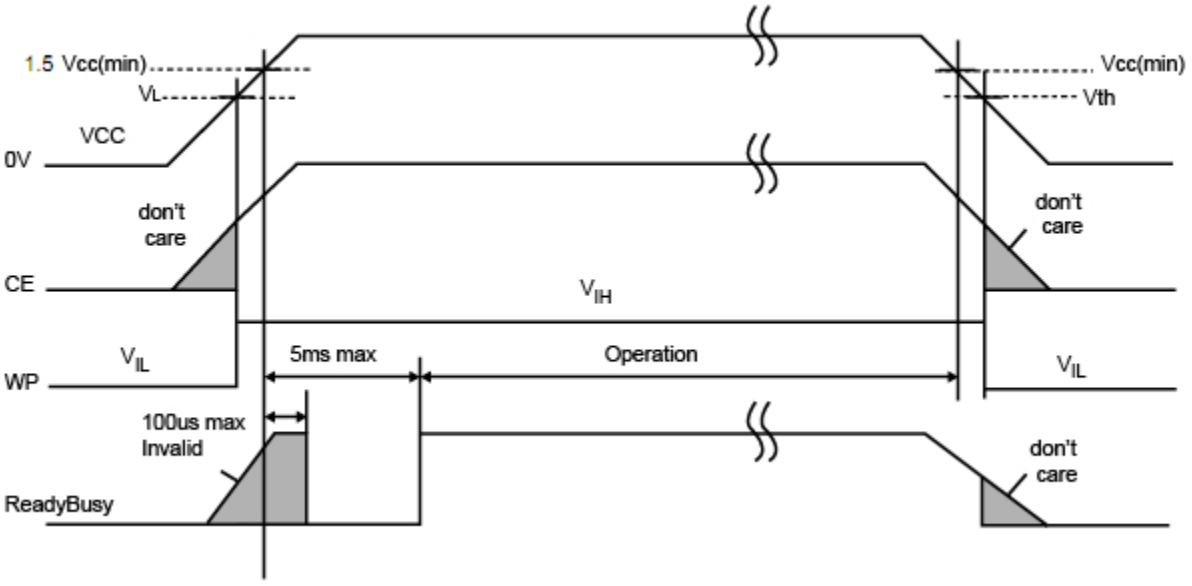
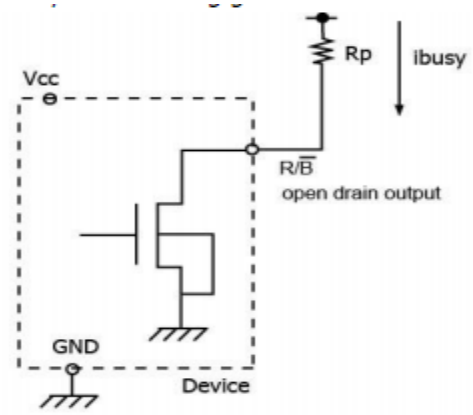


Figure 40 : Data protection and Power on/off(1.8V Device)

Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Figure 37). Its value can be determined by the following guidance.



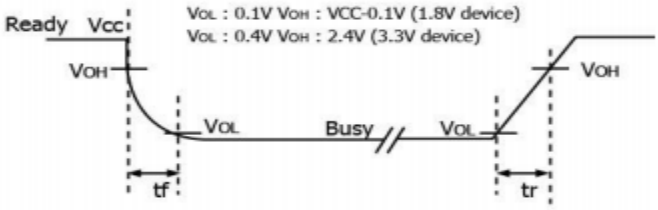


Fig. Rp vs tr, tf & Rp vs ibusy
@ Vcc = 3.3V, Ta = 25°C, CL=50pF

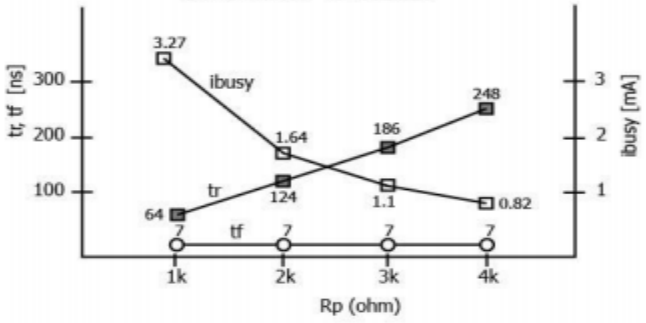
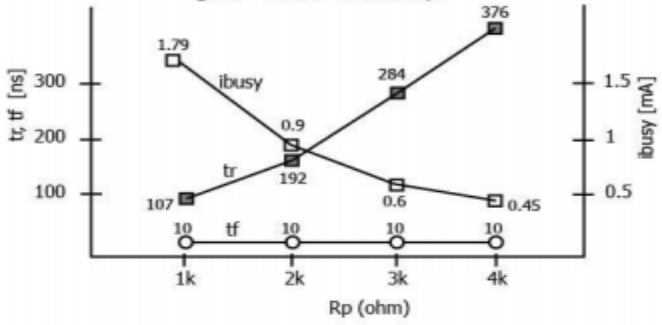


Fig. Rp vs tr, tf & Rp vs ibusy
@ Vcc = 1.8V, Ta = 25°C, CL=30pF



Rp value guidence

$$Rp\ (min\ 3.3V\ device) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \Sigma IL} = \frac{3.2V}{8mA + \Sigma IL}$$

$$Rp\ (min\ 1.8V\ device) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \Sigma IL} = \frac{1.85V}{3mA + \Sigma IL}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 41: Ready/Busy Pin Electrical Specifications

Write Protect Operation

The Erase and Program Operations are automatically reset when WP# goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows.

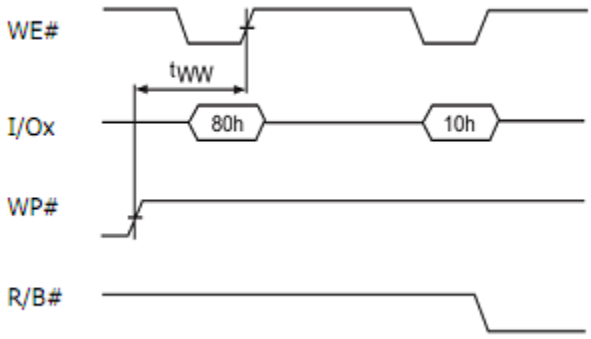


Figure 42 : Enable Programming

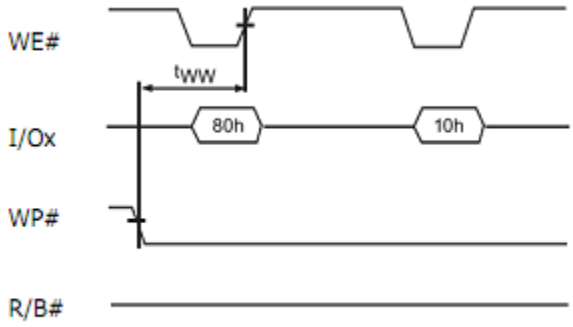


Figure 43 : Disable Programming

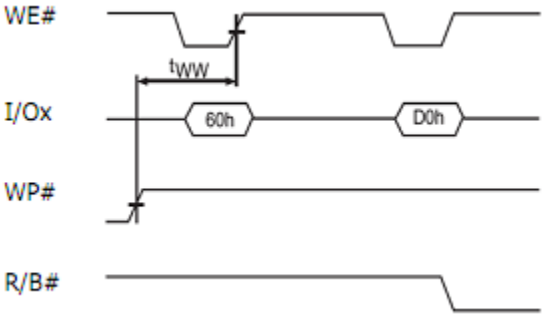


Figure 44 : Enable Erasing

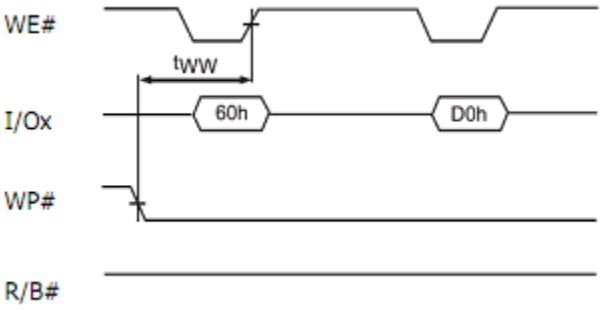


Figure 42 : Disable Erasing

8. Application notes and comments

8.1 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the First and Second page does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 43. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

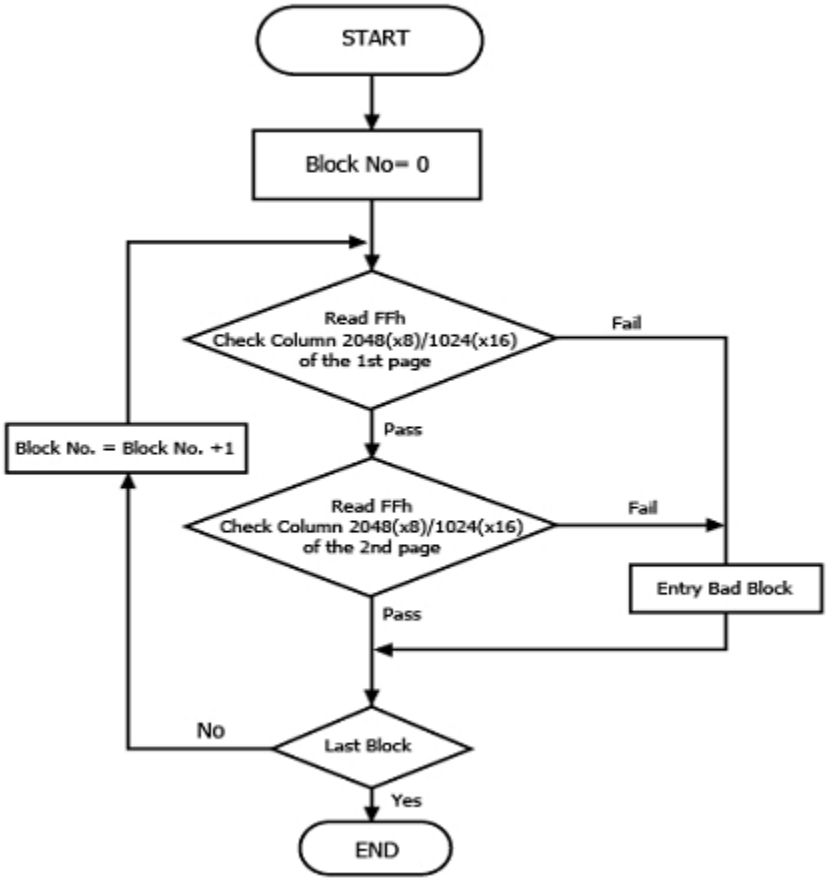


Figure 43 : Bad block management flow chart

Notes:

1. Do not try to erase the detected bad blocks, because the bad bock information will be lost.
2. Do not perform program and erase operation in invalid block, it is impossible to guarantee the Input data and to ensure that the function is normal.

8.2. Bad Block Replacement

This device may have the invalid blocks when shipped from factory. An invalid block is one that contains one or more bad bits. Over the lifetime of the device additional Bad Blocks may develop. In this case, the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block. Bad block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table 23 and Figure 44 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommanded Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC

Table 24 : Block failure

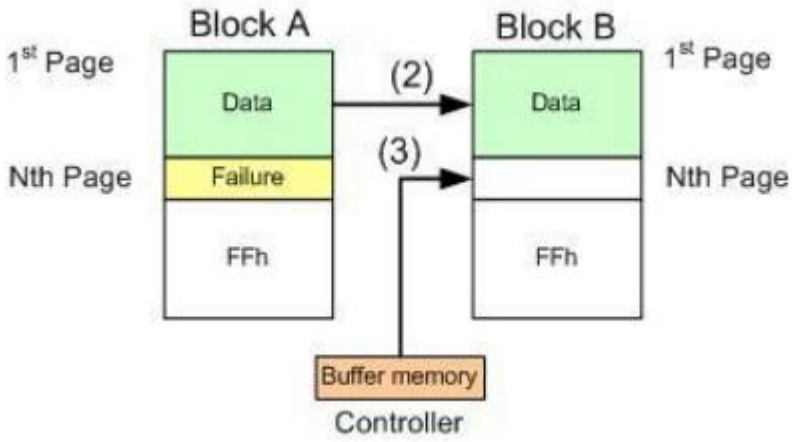


Figure 44 : Block replacement

Notes:
1. An error occurs on nth page of the Block A during Program or Erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth page of block A which is in controller buffer memory is copied into nth page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A.